INTEGRATING COUPLED MAGNETICS IN A TWO-STAGE LC LOW PASS FILTER FOR LOW RIPPLE POWER SUPPLY APPLICATIONS

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The research work was carried out under the supervision and direction of
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ABSTRACT

Electrical noise sensitive systems using mixed signal devices such as data converters and transceivers are prone to performance degradation due to switching regulator output ripple. Often switching regulator is used as power supply due to high efficiency performance it can offer. However, due to its undesirable output artefact, problems arise on powering these analog mixed signal devices directly from this regulator. Reducing the fundamental output ripple to a miniscule level is the main objective of this research. A novel concept using coupled magnetics or coupled inductors incorporated in a two-stage LC low pass filter was developed. This provides significant reduction on the fundamental frequency of switching regulator output ripple through the formation of a notch filter. However, to fully maximize the effect of the notch filter, the notch frequency should be tuned near the fundamental frequency location of the output ripple. The notch filter is created through resonance that provides better reduction of the fundamental output ripple in comparison to a conventional two-stage LC low pass filter with less volume and component count. A single package off the shelf coupled inductor can be used representing the inductors in the two-stage LC low pass filter. The resonance is formed by the mutual inductance created by the two coupled inductance and the series capacitor. Design imperfections such as the component tolerances, capacitance drift due to temperature and part-to-part coupling variations of the magnetic components are some factors that make the notch frequency hard to control. A phase-lock feedback circuit has been developed to overcome these design imperfections wherein it provides the loop correction and tuning control. A variable capacitor is used as a tuning element to align the resonant frequency with the switching frequency of the switching power supply therefore maximizing the notch filter effect to the fundamental frequency of the output ripple. Barium Strontium Titanate (BST) dielectric capacitor and off the shelf ceramic capacitor are the variable capacitors that can be used to make resonant tuning achievable.

The coupled magnetics in a two stage LC low pass filter in combination with the automatic resonant tuning concept was filed as a patent last November 6, 2017 and was issued last June 11, 2019 entitled “LC filters including coupled inductors for reducing ripple in switching power supplies” with patent no. US 10,320,280 B2. The author of this thesis is the co-inventor of the issued patent with Analog Devices Global Unlimited Co. as patent assignee.

Declaration

I hereby declare that this thesis is entirely my own work and has not been submitted for a degree in part or in full to any other University.

Aldrick S. Limjoco

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Abbreviations and Symbols

AC	Alternating Current
ADC	Analog to digital converter
ADI	Analog Devices Inc.
AVDD	Analog power supply pin
BGA	Ball grid array
BST	Barium Strontium Titanate
CIN	Input capacitor
DAC	Digital to analog converter
dB	Decibel
dBc	Decibel relative with carrier
DC	Direct Current
di/dt	Current rate of change over time
dv/dt	Voltage rate of change over time
DVDD	Digital power supply pin
EMI	Electromagnetic interference
ESL	Equivalent series inductance
ESR	Equivalent series resistance
FFT	Fast Fourier transform
FREQ	Frequency
GSPS	Giga-samples per second
IC	Integrated circuit
ILOAD	Load current
LC	Inductor-capacitor
LCR	Inductor-capacitor-resistor
LDO	Low dropout

LT	Linear Technology
MLCC	Multilayer ceramic capacitor
MOS	Metal oxide silicon
MOSFET	Metal oxide silicon field effect transistor
PCB	Printed circuit board
PFM	Pulse frequency modulation
PSMR	Power supply modulation ratio
PSRR	Power supply rejection ratio
PWM	Pulse width modulation
Q	Quality factor
RC	Resistor-capacitor
RLC	Resistor-inductor-capacitor
SFDR	Spurious free dynamic range
SMPS	Switch mode power supply
SNR	Signal to noise ratio
SOIC	Small outline integrated circuit
SSFM	Spread spectrum frequency modulation
Vc	Control voltage
VIN	Voltage input
VOUT	Voltage output
Vpp	Peak to peak voltage
VSW	Voltage on switch node
ΔIL	Inductor current ripple
ΔV	Capacitor voltage ripple

1

Introduction

1.1 Background of the study

1.1.1 Two detrimental artefacts of switch mode power supply: output ripple and switching transients

A switch-mode power supply (SMPS) or switching regulators uses semiconductor switching techniques to transfer energy from one voltage source to another and provides a regulated output voltage. It involves two storage components, inductor and capacitor which are the key passive elements of switching regulator technology [1]. However due to its switching nature, noise artefacts are inherent from SMPS. These are detrimental specially to noise sensitive systems and applications that are being powered. Thus, these degrade the overall system performance of the load if not carefully considered. Mainly, output ripple and switching transients are the two dominant undesirable noise artefacts in switch mode power supply output as illustrated in Figure 1- 1.

Figure 1- 1: Output ripple and switching transients [2]

Switching transients are high frequency voltage ringing during switching transitions of the regulator. The high frequency voltage ringing is due to the leakage current excitation of the parasitic inductance (input capacitor's equivalent series inductance or ESL plus the wire bond in the IC package) and the parasitic capacitance of the MOSFET switch within the pulsating current loop of the converter. The pulsating current loop is the loop where it generates rapid switching currents. Using a buck regulator as an example, the pulsating current loop is depicted in Figure 1- 2. The red dashed box is the loop where the current is rapidly switching discontinuously (high di/dt or high current rate-of-change) during switching transitions. Figure 1- 3 illustrates the voltage switch node and transistor current waveforms.

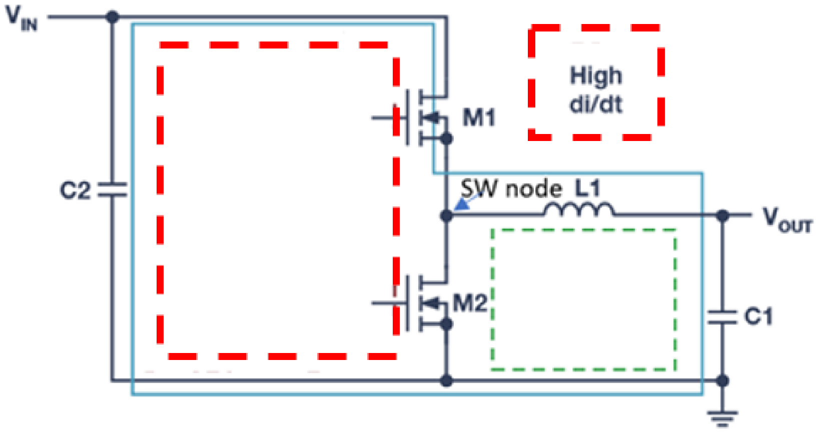

Figure 1- 2: Buck regulator current loops [3]

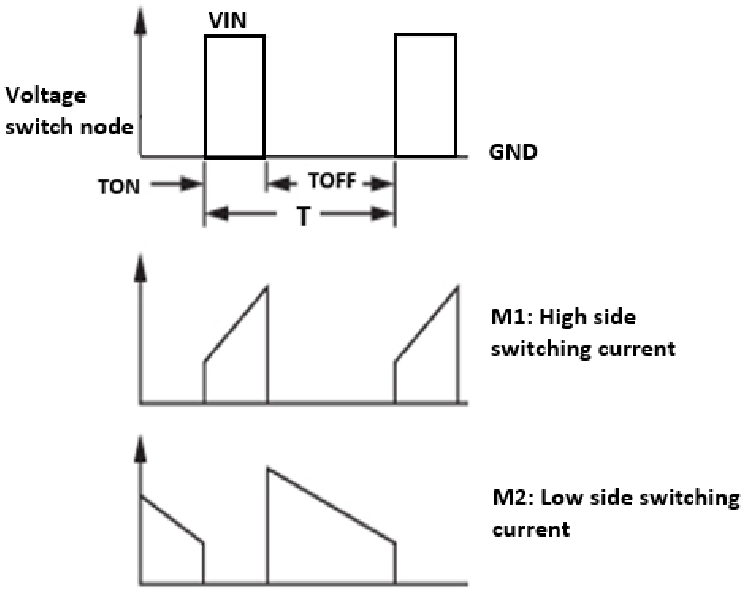

Figure 1- 3: Buck regulator switch voltage and current waveforms

The high frequency voltage ringing is caused by the resonance formed between the parasitic inductance and parasitic capacitance within the pulsating current loop [4]. PCB (printed circuit board) layout traces is also a factor that adds up on the overall parasitic inductance. These become worst with bad lay-out design comprising larger current loop area. A good practice in PCB lay-out is to design the pulsating current loop area as small as possible reducing the overall loop parasitic and trace inductance as seen in Figure 1-4.

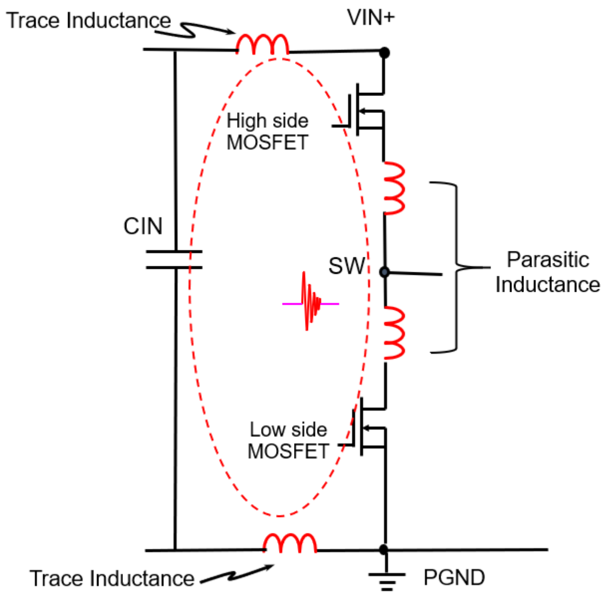

Figure 1- 4: Trace parasitic inductance in pulsating current loop

The body diode reverse recovery current (leakage) of the MOSFET that ensues during dead time excites these parasitic effects. In effect, it creates the voltage ringing on the switching edges. This increases with faster switching speeds. The same goes to the falling edge ringing that are created through the resonant parasitic of the loop encompassing the low and high side MOSFET. These voltage overshoot and undershoot at the switch node can parasitically couple at the output of the SMPS through the parasitic capacitance across the storage inductor and parasitic inductance in series with the output capacitor. The noise artefact occurs at very high frequencies and is a classical manifestation of an electro-magnetic interference (EMI). These can be mitigated by slowing down the switching transitions or designing a damping network with the expense of lowering the SMPS efficiency [5]. Another approach is by using an external filter at the output rail of the switching regulator such as ferrite bead [6]. This filters high frequency noise energy by utilizing its resistive region over an intended or target broad frequency range.

The other nuisance in switching power supply is output ripple. Output ripple is the output voltage fluctuations due to the charging and discharging of output capacitor by the inductor current ripple. The characteristic and amplitude of output ripple depends on the regulator's topology, duty, switching frequency and type of external components used such as output capacitor (considering equivalent series resistance or ESR and capacitance) and inductor (inductance) [7]. The output ripple is predictable and coherently related to the switching frequency of the SMPS specifically when operating in pulse width modulation.

1.1.2 Estimating output ripple

Figure 1- 5 shows a simplified buck regulator operating in a steady state condition.

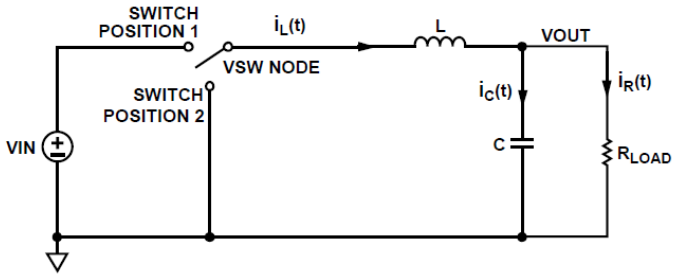

Figure 1- 5: Simplified buck regulator configuration [2]

Two switches (high side and low side MOSFET for synchronous buck) can be in switch position 1 and switch position 2. A single pole double throw switch was used to represent the two switches for simplicity. When switch1 is closed and switch 2 is open, the voltage difference between VIN and VOUT at steady state is imposed across the inductor and the inductor current ramps up. When switch 1 is opened and switch 2 is closed, the voltage at VOUT is imposed across in the inductor but with a change of direction of the current as the inductor now sources the current. The inductor current ramps down as seen in Figure 1- 6.

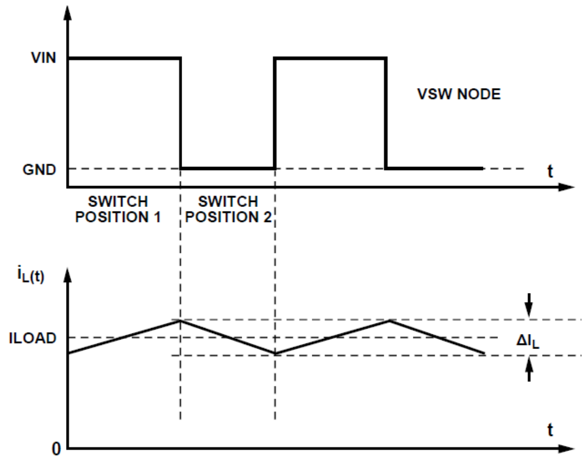

Figure 1- 6: Switch node voltage and inductor current waveform [2]

The DC load current flows through the load while the inductor current ripple flows through the capacitor with the assumption its impedance at the switching frequency is much lower than the impedance of the load. The inductor current ripple charges and discharges the output capacitor therefore generating an output voltage ripple.

Figure 1- 7 illustrates the capacitor current and capacitor voltage waveform of a buck converter.

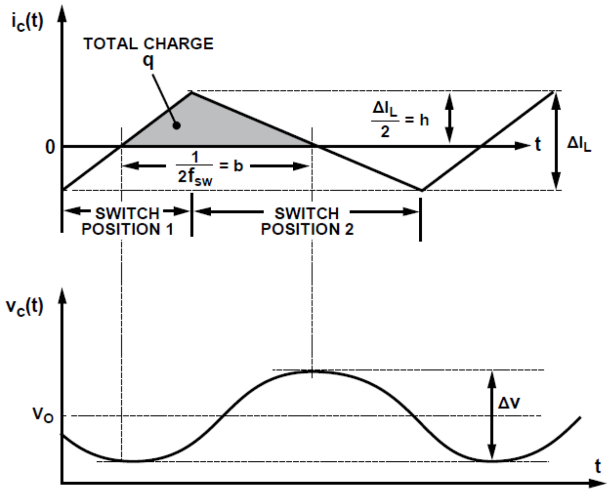

Figure 1- 7: Capacitor current and voltage waveform [2]

The output voltage ripple can be associated on the positive (shaded) portion of the capacitor current waveform. The capacitor current waveform consist of the inductor current ripple without the DC load current. Charge is being stored in the capacitor plates during the positive portion of the capacitor current waveform. This provides half of the complete cycle of the switching frequency where capacitor voltage changes between its minimum and maximum values. The total charge on the positive portion of the capacitor current waveform is:

$$q = C\ (\Delta \mathrm{v}) \tag{1}$$

Where charge q is the integral of the current waveform between its zero crossings, C is the capacitance and Δv is the voltage output ripple. This can be expressed as an area of a triangle using base as 1/(2fsw) and height as ΔIL/2. ΔIL is the inductor current ripple from peak to peak and fsw is the switching frequency of the converter. The total charge q can be expressed as:

$$q = \frac{b\ x\ h}{2} = \frac{(\Delta IL)}{8\ x\ fsw} \tag{2}$$

Solving the output voltage ripple yields

$$\Delta v = \frac{\Delta IL}{8\ x\ fsw\ x\ C} \tag{3}$$

Therefore, inductor and output capacitor are the main components that directly affect output ripple. Inductor current ripple (ΔIL) is inversely related to the inductance (L).

Other components affecting inductor current ripple are the input voltage (*VIN*), output voltage (*VOUT*) and the switching frequency (*fsw*) [7]. These can be seen from (4):

$$\Delta IL = \frac{VIN - VOUT}{L\ x\ fsw}\ x\ \frac{VOUT}{VIN} \tag{4}$$

Output ripple is an important design consideration in switching power supply. For a typical buck regulator, increasing the storage inductance and output filter capacitance can dramatically lower the output ripple. However, the size of the magnetic and the number of output capacitors can come at the expense of board space and cost [7]. In addition, using large inductor and capacitor component values lead to a slower transient response which places the inductor-capacitor pole at lower frequency constituting a slower loop bandwidth. Increasing the switching frequency on the other hand, can reduce the voltage output ripple but at the expense of lower efficiency due to its high occurrences of switching or transitional losses [8]. Hence, increasing the output capacitance and storage inductor too much is impractical. Sometimes power system design also requires an additional stage LC filters or a low drop-out (LDO) regulator with high power supply noise rejection, cascaded after the switching regulator to filter the output ripple to an acceptable level [9]. The cons are additional components which constitutes to an increased board space and cost.

In some cases, switching power supplies are often replaced with LDO's. LDO has cleaner output spectrum because it uses linear and non-switching techniques to regulate the output voltage. However, it is inefficient because it dissipates power across the pass element. Hence if the input to output differential (headroom voltage) is large, it induces higher power loss across the pass element which linearly increases at higher load currents.

1.1.3 Output ripple effects on analog signal processing components

Effects on high speed digital to analog converter (DAC)

This section demonstrates the effect of power supply ripple to giga sampling per second digital-to-analog converter (GSPS DAC). The DAC part used in this section is AD9175 that comprises two analog (AVDD1.0, AVDD1.8) and two digital (DVDD1.0, DVDD1.8) power supply rails [10]. The most sensitive rail is the 1V analog supply rail and this was determined by characterizing its AC power supply rejection ratio (AC PSRR) and power supply modulation ratio (PSMR). AC PSRR represents the ability of the DAC to reject the power supply ripple on the power supply pin over a range of frequencies while similarly, PSMR represents the ability of the DAC to reject the power supply ripple in the presence of a carrier signal or data being processed [11]. The PSMR represents an accurate application environment. Figure 1- 8 shows the maximum allowable ripple results for 1V Analog supply rail (DAC output 1 channel) superimposed to the output spectrum of a buck regulator, LT8650s [12]. LT8650s is a Silent Switcher® product from Analog Devices Inc. that uses novel design and packaging techniques which virtually eliminates high frequency voltage ringing during fast switching edge transitions [3]. The high frequency voltage ringing translates as an EMI problem. Conventional techniques on reducing high frequency voltage ringing are achieved by slowing down the switching transitions or adding a snubber circuit but at the expense of lower efficiency and additional component space. However, Silent Switcher® allows to attain higher efficiency without the use of these conventional techniques while still substantially reducing the EMI level. Conversely, fundamental ripple due to charging and discharging of output capacitor by the inductor current ripple is still apparent.

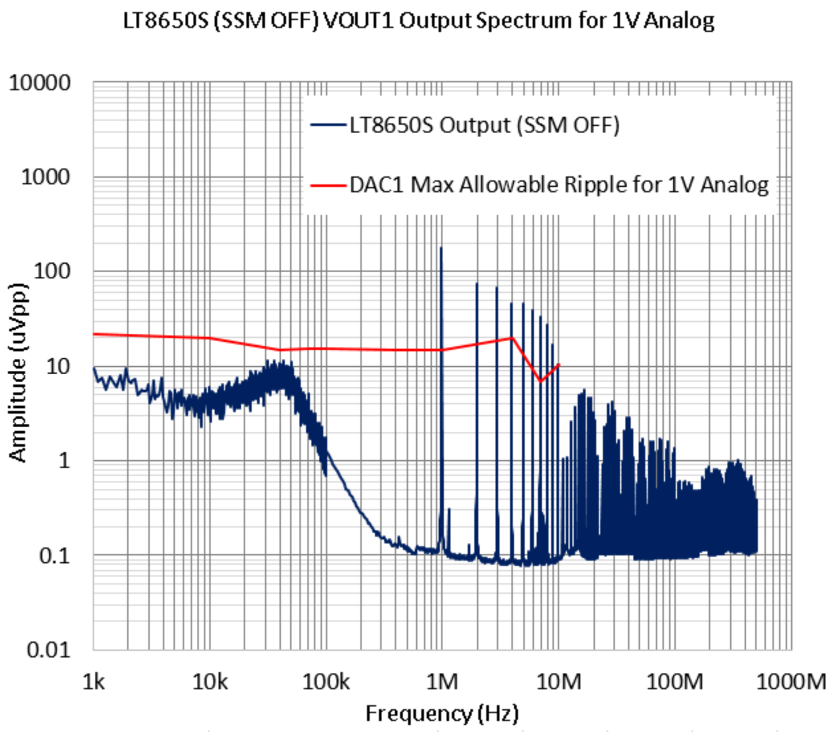

Figure 1- 8: Buck regulator output spectrum vs. maximum allowable ripple threshold

The switching spurs of the buck regulator exceeded the maximum allowable ripple level threshold. This resulted modulated sideband spurs around the DAC carrier signal as seen in Figure 1- 9 which is detrimental to the part phase noise performance.

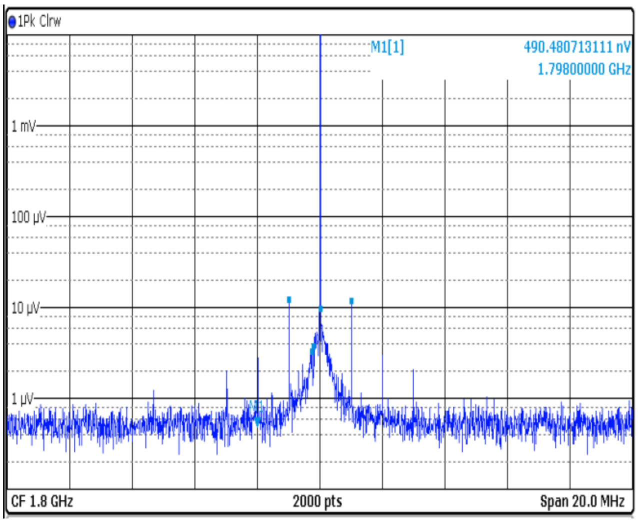

Figure 1- 9: DAC output spectrum with modulated sideband spurs

The maximum allowable ripple level threshold was derived from acquiring the PSMR data. Figure 1- 10 shows the block diagram of the AD9175 PSMR test bench set-up. The test bench set-up is referenced from the work of Reeder, “Designing Power Supplies for High Speed ADC” [11].

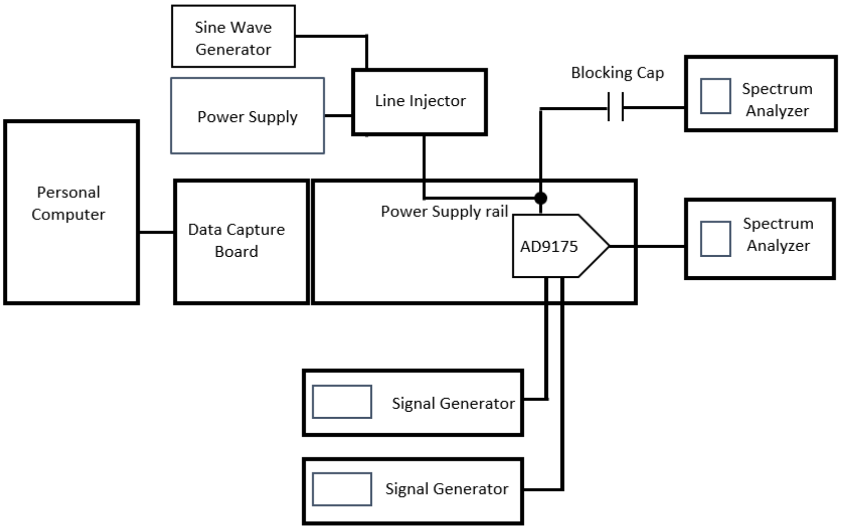

Figure 1- 10: PSMR test set-up

An emulated power supply ripple is achieved through combining the sinusoidal signal from a waveform generator and a clean DC power supply source using a line injector. The line injector is a summing amplifier that combines the DC and AC signal components.

The output of the line injector is applied to the analog input power rail (AVDD1.0 for example) of the DAC. A spectrum analyser is used for measuring the peak amplitude of the injected sinusoidal signal on the power rail. Parasitic inductance created by the board traces can act as an added filter. This increases the rail impedance for high frequency AC currents. In order to get an accurate measurement, probing directly on the analog input pin for the spectral measurements is required. The probe point should be on the pads underneath the BGA package of AD9175. The AD9175 DAC output is also connected to another spectrum analyser for measuring the related injected spurs from the supply input. Figure 1- 11 shows the spectral data of the DAC output wherein spurs appeared both sides of the carrier signal. A good power supply ripple rejection should ideally have very low to zero amplitude spur appearing on the output in contrast from the larger amplitude of the injected ripple.

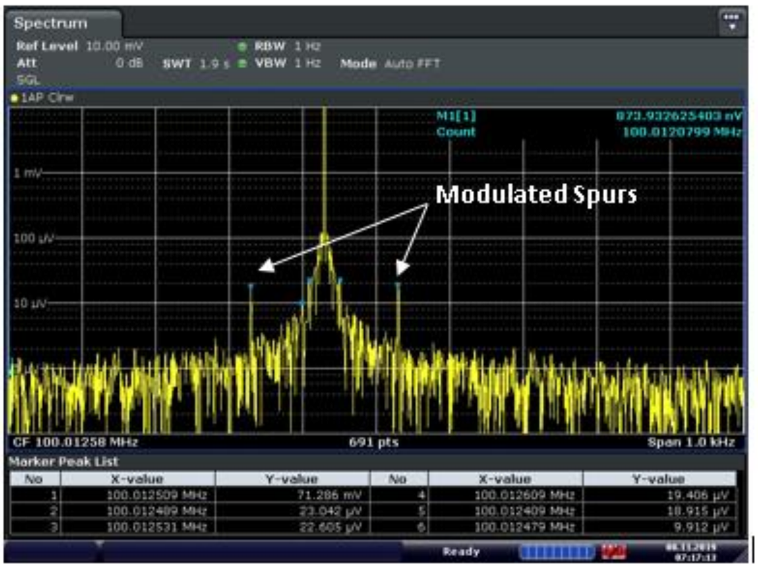

Figure 1- 11: Modulated side band spur around the carrier signal

PSMR can be determined by calculating the ratio of the injected ripple amplitude measured at the power supply pin to the modulated sideband spur amplitude formed around the carrier signal measured at the DAC spectrum output seen in (5).

$$PSMR\ (db) = 20 \log \frac{injected\ ripple\ amplitude}{modulated\ spur\ amplitude} \qquad (5)$$

Figure 1- 12 show the PSMR results for AVDD 1.0V rail, for DAC1 with carrier frequencies across 100 MHz to 3600 MHz. DAC clock rate used is 5.89824 GHz and injected ripple frequencies on the supply rail range from 10 kHz to 10 MHz. Results show that the 7 MHz ripple frequency has the lowest PSMR. For analog output frequency or f_{OUT} of 100 MHz to 1800 MHz, PSMR decreases from 41 dB to 17 dB respectively.

Increasing the analog output frequency to 3600 MHz (created a 2300 MHz fold over frequency) has increased PSMR to 20 dB mark.

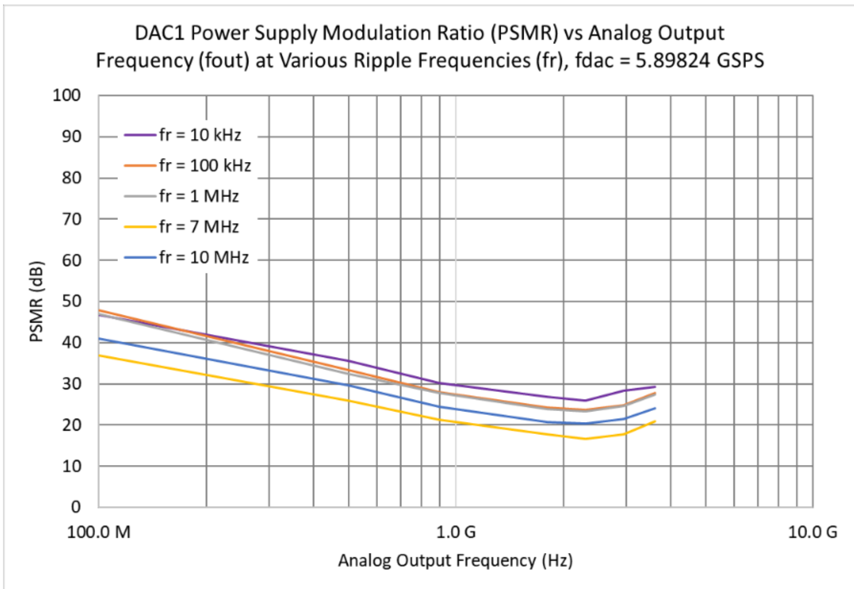

Figure 1- 12: AVDD1.0 rail PSMR vs analog output frequencies at various ripple frequencies for DAC

From the PSMR results, the maximum allowable ripple can be determined depending on the criteria set such as SFDR limits, average noise floor or percentage fraction of an LSB. In the plots shown in Figure 1- 13, the 1.0 µVpp noise floor on the DAC output spectrum is used as a criterion. The equation below shows the relationship of PSMR (dB) with the maximum allowable input ripple (V_{R_MAX}).

$$V_{R\_MAX} = \left[10^{\frac{PSMR\ (dB)}{20}}\right] \times Noise\ Floor \qquad (6)$$

Carrier frequencies near the Nyquist (1800 MHz, 2300 MHz, and 2950 MHz) have the lowest PSMR and thus translated to lowest maximum allowable ripple. The maximum allowable ripple at 100 Hz to 4 MHz is approximately 15 µVpp. The lowest PSMR is at 7 MHz in which maximum allowable ripple is approximately 7 µVpp. Thus AVDD 1.0V power rail is sensitive to power supply ripple and post filtering is required to filter the spurs appearing on the DAC output spectrum. The worst maximum allowable threshold for analog output frequency of 2.3GHz is used on Figure 1- 8.

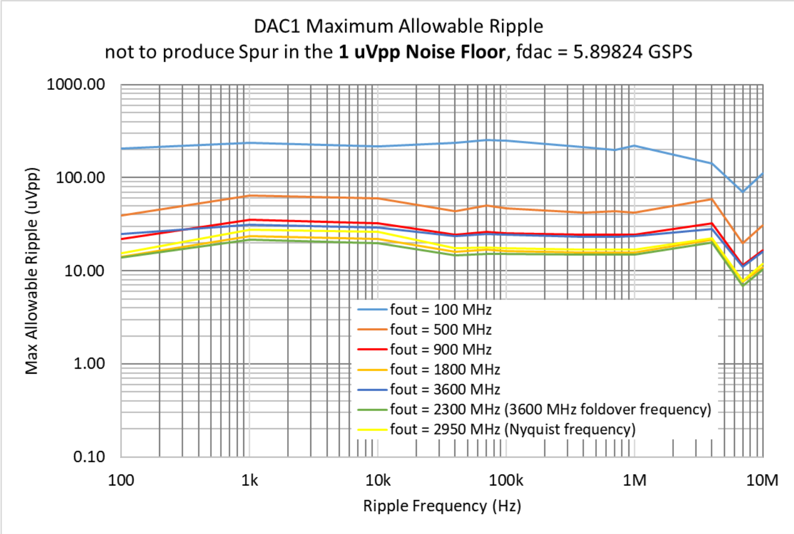

Figure 1- 13: AVDD1.0 rail maximum allowable ripple not to produce spur above the 1 µVpp output spectrum noise floor for DAC

Effects on high speed Analog to Digital Converter (ADC)

High resolution and high speed ADC are also prone to switching power supply output ripple. Output ripple can appear as a distinct spur on the ADC output spectrum. Worst, this can also generate modulation spurs around the carrier signal and degrade the signal to noise ratio (SNR) and spurious free dynamic range (SFDR) parameters [13]. Figure 1- 14 shows measured FFT test results of a 12-bit GSPS ADC with 56 dB SNR and 80 dBc SFDR specifications being powered by a buck regulator. Spurious sidebands of 670 kHz and 1340 kHz are being generated around the carrier signal. These are due to the modulation between the analog input carrier (signal being digitized) and the voltage output ripple running at switching frequency of 670 kHz. The generated sidebands resulted a decreased SNR and SFDR performance by 2 dB.

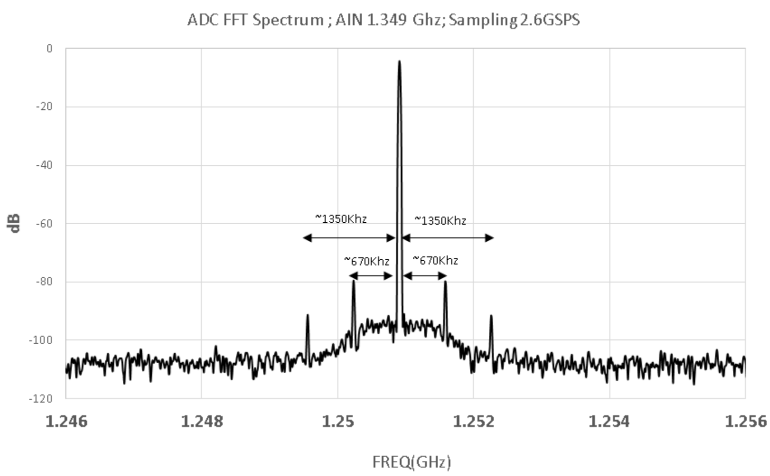

Figure 1- 14: ADC FFT zoom view of analog input carrier signal

This is unavoidable as more systems require higher performance and higher resolution signal processing converters. Therefore, this implies that noise sensitive system becomes more susceptible to the switching regulator output ripple artefact.

Effects on wideband RF transceiver

Similar effect was also seen for integrated dual wideband RF transceiver, ADRV9009 from Analog Devices Inc. [14]. The DC-DC regulator is an Analog Devices Inc., LTM8075 power µModule using Silent Switcher technology with spread spectrum enabled [15]. Spread spectrum frequency modulation (SSFM) technique uses triangular frequency modulation at a rate of approximately 3 kHz that continuously varies the switching frequency over a range covering the programmed switching frequency value to about 20% higher than that value [15]. In effect it lowers the peak amplitude of the ripple at the converter's fundamental operating frequency. This is a useful advantage but generates low frequency spurs related to its triangular frequency modulation. This brings some drawback on the performance for applications that have low power supply rejection at low frequencies. In contrast to pulse width modulation with disabled spread spectrum, no modulation spur will be apparent at low frequencies. Figure 1- 15 plots the output spectrum of the switching regulator running with spread spectrum enabled. The dashed line is the maximum allowable ripple for one of the power supply pin (VDDA) 3.3V of the transceiver part wherein it can still tolerate. The VDDA 3.3V is the power supply domain for analog and clock circuitry of the transceiver. The first three modulation frequency spurs exceeded the allowable threshold which resembles as modulated side band spurs around the RF carrier as shown in Figure 1- 16. In this case phase noise performance of the transceiver part can be severely affected.

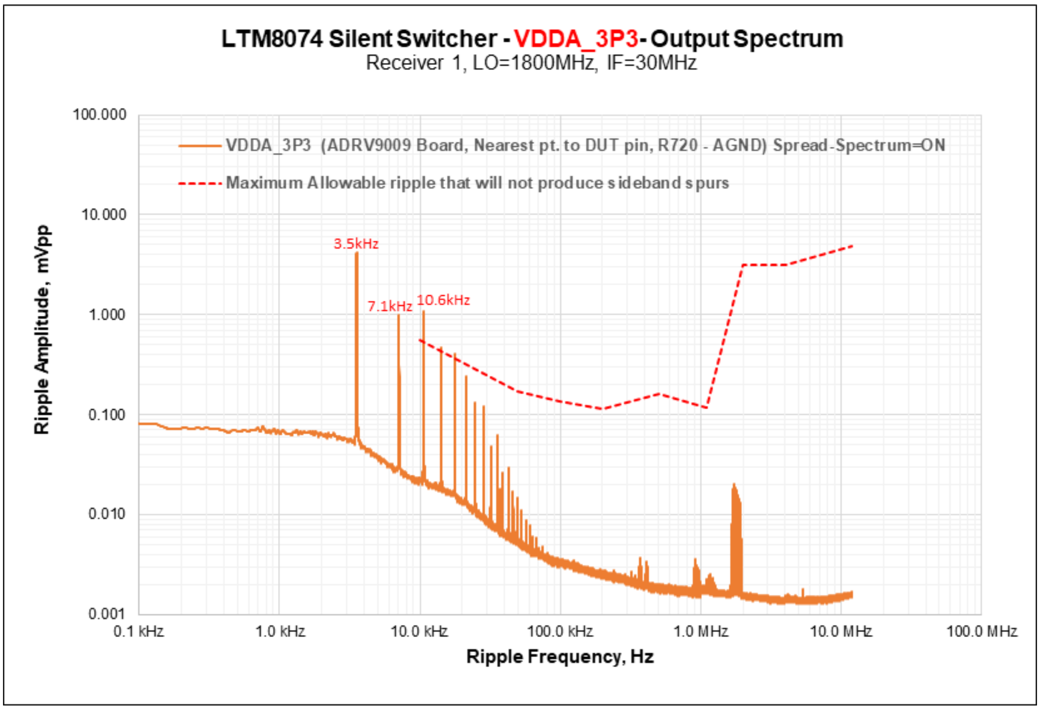

Figure 1- 15: Switcher output spectrum enabled spread spectrum vs. maximum allowable ripple in analog supply input of transceiver

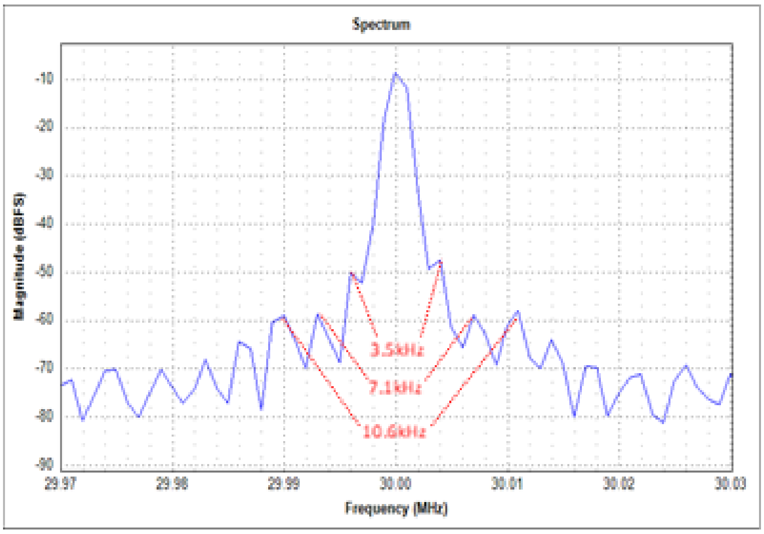

Figure 1- 16: Modulated sidebands caused by the triangular modulation frequency

The key advantage of SMPS or switching regulator is therefore high efficiency. Overall power loss is significantly lesser compared to linear or low dropout regulators. This is crucial in system design which requires longer battery life and better thermals which eliminates the use of large heat sinks.

1.2 Motivation

The project aim is to develop a compact output filter solution with very high attenuation at the fundamental output ripple frequency. Mitigation of switching transients during switching transition will not be covered on this paper. The use of coupled magnetics or coupled inductors in a two-stage LC low pass filter can provide significant reduction on switching power supply output ripple. This can be done through the formation of a notch filter that can be tuned near the exact frequency location of the fundamental output ripple. It provides high ripple attenuation due to series resonance effect. Coupled magnetics in a two stage LC filter provides greater reduction on the output ripple in comparison with conventional filters with lesser volume and component count.

1.3 Thesis overview

Chapter 2 begins with an overview of existing filtering techniques on switching regulator output ripple. This provides related literature which involves passive and active methods of filtering. Passive filters such as using ferrite beads and the conventional LC filter were discussed and how these filters can be used to attenuate the fundamental output ripple. Some related literature in regards the use of resonance as an effective ripple filtering technique were also shown. Another method of filtering power supply ripple shown in this chapter is using low drop-out regulator (LDO). An active filter technique utilizing its inherent power supply noise rejection to suppress the unwanted switching power supply noise artefacts. Load current and voltage headroom (input to output differentials) are some of the key aspects that are discussed in the chapter which dramatically affects the power supply rejection ratio (PSRR) performance.

Chapter 3 presents a novel way of using resonance to significantly attenuate the fundamental output ripple from switching power supplies. The introduction of coupled-magnetic filter was discussed and how this can be implemented in a conventional two stage LC low pass filter. An automatic resonant tuning design using phase lock loop was introduced to utilize the notch filter and automatically aligns the given notch frequency to the fundamental output ripple frequency. The use of variable capacitance components such as barium strontium titanate (BST) dielectric capacitor or multi-layer ceramic capacitor as tuning element enables the possibility of resonant tuning.

Chapter 4 demonstrated the experimental platform comprising all the required components to build up the auto tuning circuit. This was designed and implemented in a

PCB prototype. The schematic design and lay-out details was shown in the chapter. In addition, aspects on electrical specifications, bonding diagram and proto-typing of BST capacitor in a SOIC package were also presented.

Chapter 5 details the various tests that were carried out to verify that the functionality of the design. The coupled-magnetic filter in a two stage LC low pass filter works as intended and the manifestation of the notch filter based from the configuration shows that it is an effective output ripple filter approach. This was tested on an actual buck regulator and it resulted an extremely low voltage output ripple after the said filter. Resonant phase detection and tuning test was also conducted in an open loop configuration. All results are recorded and organized in this chapter.

Chapter 6 is the concluding chapter which summarizes the complete research process about the implementation of coupled inductor filter technique in a two stage LC low pass filter. Future work recommendations are included in the chapter to further improve the resonant auto-tuning concept.

1.4 Contribution

The original contribution of the thesis can be summarized as follows:

a. The thesis introduces a novel idea of using an auto-tune coupled-magnetic resonant filter in a two stage LC low pass filter to significantly reduce the fundamental output ripple from switching regulators. Resonance is established using the mutual inductance element of the coupled magnetics together with the variable capacitor wherein it can be a Barium Strontium Titanate dielectric or an off the shelf multi-layer ceramic capacitor. An auto tuning phase detection circuit was designed to automatically align the resonant frequency of the coupled-magnetic filter to the fundamental frequency of the output ripple of the switching regulator.

b. A patent was filed and issued covering the concept of automatic resonant tuning using coupled-magnetic filter to reduce output ripple on switching regulators with the author of this thesis as a co-inventor. The patent no. is US 10,320,280 B2 entitled "LC filters including coupled inductors for reducing ripple in switching power supplies".

2

Literature Review

2.1 Passive filters

Electrical filters plays a vital role in power system design using switching regulators. This reduce any voltage variations caused by the switching nature of the switching regulators in order to provide a much stable and cleaner output voltage. Electrical filters often uses passive components. An example are ferrite beads. These are passive filters that serves the purpose for filtering high frequency noise. The bead becomes resistive over the frequency of interest and dissipates the noise energy in the form of heat. Ferrite bead is usually connected in series with the power supply and combined with decoupling capacitors to form a low pass filter network. This is effective on filtering EMI and often used in each power rails for high frequency noise isolation [16]. Figure 2- 1 shows an example.

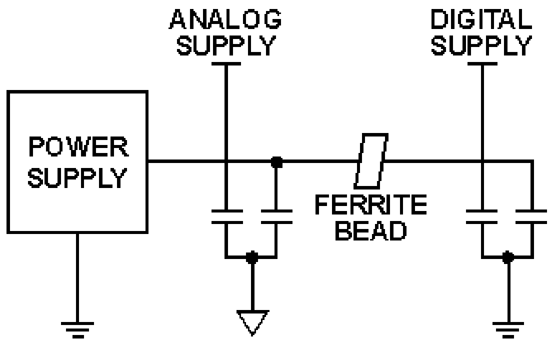

Figure 2- 1: Ferrite bead implementation [17]

However, ferrite bead is very effective in filtering high frequency noise such as the high frequency voltage ringing that is being produced during the switching transitions of switching regulator. On other hand, it is not relatively effective in filtering the output ripple where it occurs on a much lower frequency. An example of impedance vs frequency curve of a ferrite bead with its reactance(X), resistance(R) and impedance(Z) is depicted in Figure 2- 2.

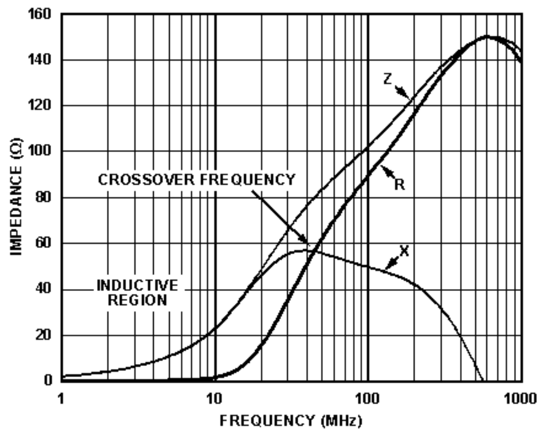

Figure 2- 2: Impedance curve [17]

In most cases, switching regulators usually operates at switching frequency below 5 MHz. The plot shows that the impedance within the frequency operation range of switching regulators is not high (less 20Ω) compared to the impedance of the bead where it becomes almost equivalent to its resistance (approximately 150Ω). High impedance is seen from 300 MHz to 1 GHz which ferrite bead becomes an effective EMI suppressor. But with the combination of decoupling capacitor, there will still be some level of attenuation below 5 MHz depending on the bead's inductance and capacitor's capacitance values. The values of these two reactive components dictates the 3 dB pole or cut off frequency. In addition, key considerations in using ferrite beads should also be accounted for. First, there are large variation of impedance across DC load current. This should be carefully considered when choosing ferrite beads depending on the various application demands of supply current levels. High current can cause saturation of the ferrite material and produce significant change on its effective impedance [16]. Figure 2- 3 shows how increasing load current decreases the effective impedance across the specified frequencies.

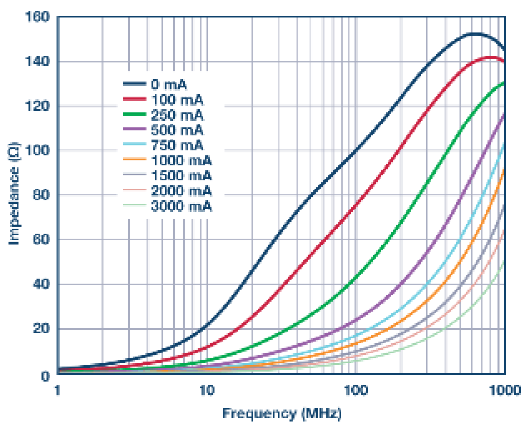

Figure 2- 3: Impedance curve vs. DC bias currents [16]

Second is the series resonance due to the inductance of the bead and the decoupling capacitance, especially, when the capacitor has very low ESR such as MLCC or multi-layer ceramic capacitor. Figure 2- 4 shows an insertion loss or forward transmission characteristic of a ferrite bead and high Q (low ESR) ceramic capacitor. There is a gain (peaking) around 1 to 3.5 MHz frequency range which is not desired. This is detrimental in a system because it can amplify noise in the specified frequency range instead of attenuating it.

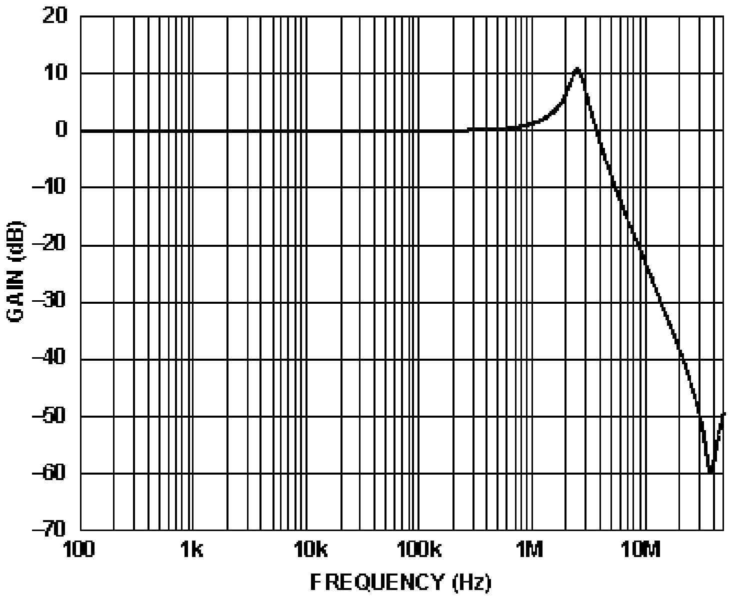

Figure 2- 4: Forward transmission characteristic [17]

Another conventional low pass filter for switching regulators employs passive components such as inductor (as series element) and capacitor (as shunt element). Design goal is to maximize the series impedance and minimize the shunt impedance for the target frequency range. One example from the work of Limjoco et al, “Silent Switcher Quietly Power GSPS ADC in Half the space”, an inductor of 1.2 µH was added as a series element to increase the attenuation of the fundamental ripple at 1 MHz range as shown in Figure 2- 5 [18].

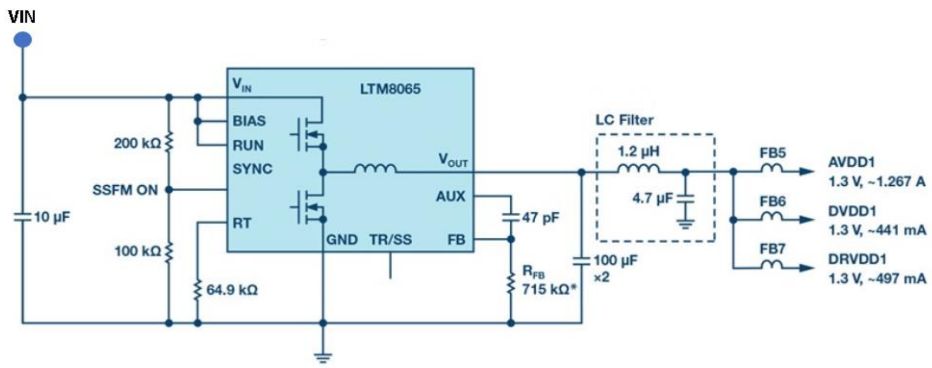

Figure 2- 5: Switching regulator using post LC filter [19]

Figure 2- 6 shows a reduction of 25dB on the fundamental frequency of the output ripple. This constitutes that adding a series inductor in combination with shunted capacitors will provide a two pole low pass filter with 3dB cut-off frequency depending on the inductor and capacitor values. In this case the cut-off frequency is 67 kHz.

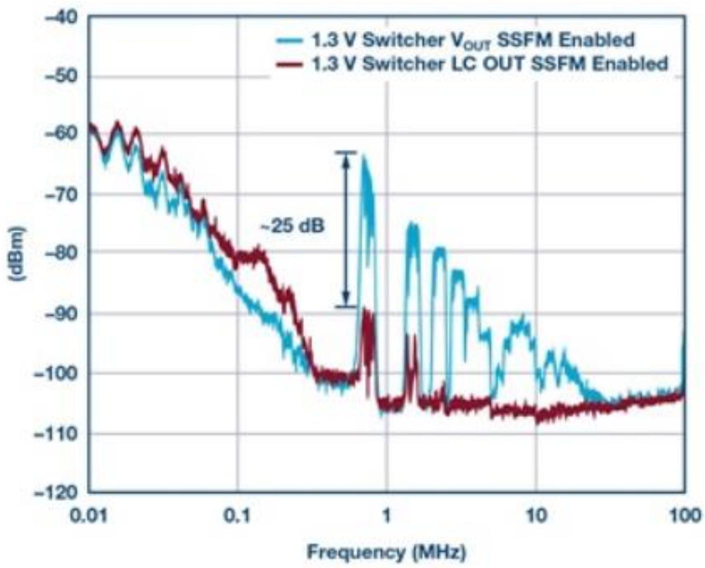

Figure 2- 6: Switching regulator output spectrum with and without an LC filter [19]

Another example of using LC filter is the work of Ridley (Second-Stage LC Filter Design) [20]. Adding a second stage LC filter after the storage inductor and capacitor of a switching power supply can significantly reduce the output ripple. In contrast with single stage LC filter, the second stage LC filter is far better because components can be designed to be smaller with the same amount of attenuation or it does not take substantial increase in filter volume to increase the attenuation performance. However careful design considerations must be observed to avoid stability problems. The resonance of the single stage should be inside the feedback loop while the second resonance of the second stage must be above the control loop crossover frequency. In addition, damping elements are also required to minimize the peaking effect. Another factor to consider is the capacitive loading. Designing the second capacitor 2-20x larger than the first capacitor eliminates any capacitive loading effects. Following these design considerations are critical to achieve good stability, better filter performance and volume. In view of the coupled-magnetics approach with the use of resonance, this generates a narrow band deep attenuation response and is far superior to a conventional two stage LC low pass filter in terms of filtering a single distinct ripple frequency.

Resonance is found to be useful in filter applications as revealed by Meehan Et al (Varactor–Based Passive Ripple Filter with Automatic Tuning for Low-Noise Power Supply Systems) [21]. The use of tank resonance is proven effective in power supply ripple filtering if the fundamental ripple frequency coincide with the tank resonance. The difficulty in aligning the resonance on the ripple frequency fundamental due to component manufacturing tolerances are addressed by an automatic tuning control using BST (Barium Strontium Titanate) capacitor as the tuneable element. BST capacitors are tuneable capacitor wherein its capacitance can be varied by applying voltage across it. Similarly, on the coupled-magnetic filter concept in a two stage LC low pass filter, view as another resonant filter approach utilizing the roll-off of a two stage LC filter in addition to its notch effect at discrete frequency.

Coupled-Magnetic Filters with adaptive inductance cancellation by Lymar et al. has shown the use of coupled-magnetics in filter applications [22]. This enable high order filter structure to be realized with the use of a single magnetic component. However parasitic shunt inductance due to imperfectly magnetic coupling negates the high order filtering ability. This limitation is overcome by an adaptive inductance cancellation control with feedback based on the sensed output ripple. This technique eliminates the shunt parasitic inductance of the magnetic coupling mismatch and the parasitic inductance of the capacitor by using a trimmer inductor. This bring the overall shunt path inductance to zero, therefore preserving the high order filter structure without substantial increase in filter size and cost. In view of the coupled magnetics in a two stage LC filter, the approach is different. Instead of cancelling the shunt inductance, the mutual inductance was used to form a series resonance with the shunt capacitor creating a notch filter effect.

2.2 LDO as post regulator filter

LDO are commonly employed to post regulate and filter the output noise artefact at certain frequency extent of switching regulators. In contrast with passive filters, some advantages are voltage accuracy, stability and good transient response. A basic schematic of an LDO is seen in Figure 2- 7.

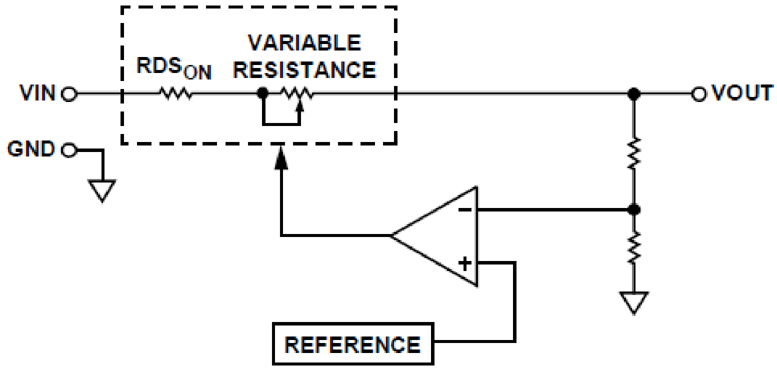

Figure 2- 7: Simplified LDO schematic [23]

The error amplifier compares the stable reference voltage with the divided down fraction of the output voltage. This then controls the gate of the pass element which is represented as a variable resistance to regulate the output voltage with respect to input voltage and load perturbations.

Besides the advantages, LDO has inherent power supply rejection ratio (PSRR) in which the open loop gain is the dominant factor [24]. PSRR is basically a measure how well the circuit suppresses or rejects power supply noise on the supply input to keep off on corrupting the output voltage.

LDO PSRR is a function of frequency. Figure 2- 8 shows the three domains of PSRR.

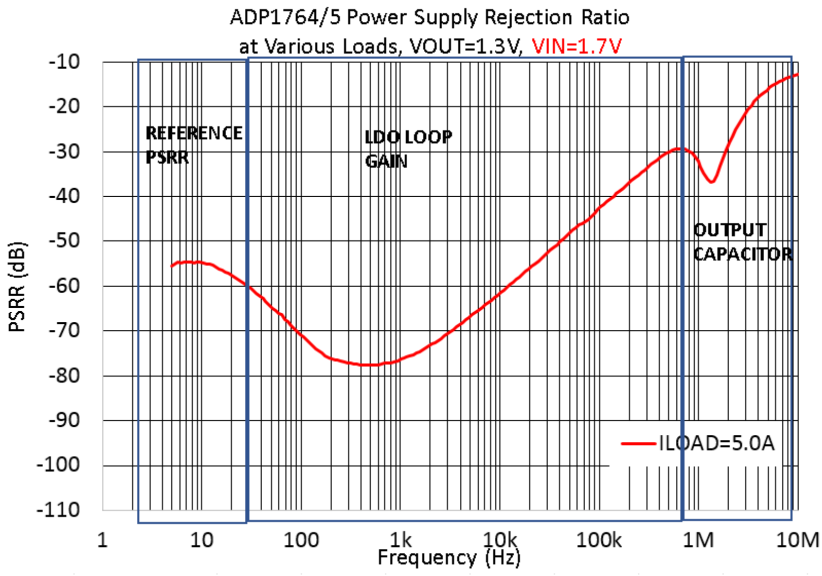

Figure 2- 8: LDO PSRR region

The PSRR ranges below 30Hz is highly dependent on the bandgap reference and the open loop gain. The second region is dominated with the open loop gain of the error amplifier. At low frequencies, the AC gain of the error amplifier is equal to DC gain until it reaches its 3dB cut-off. By then, AC gain continuously to roll-off until it reaches its unity gain bandwidth. The open loop gain decreases with frequency and so its power supply rejection. Above the unity gain frequency, the error amplifier has little control over the PSRR, therefore, the dominant factor are the output capacitor and any parasitic from input voltage to output voltage path [25]. It can be seen on the plot from 600 kHz to 1.5 MHz, the output capacitance provides the increasing PSRR until it reaches its self-resonance (1.5 MHz). Then the PSRR decreases as the ESL of the capacitor dominates.

Moreover, LDO PSRR is also a function of load current and voltage headroom [23]. Load current affects the open loop gain of the error amplifier and therefore its PSRR. At light loads, the impedance of the pass element is much higher. The pole formed between the output capacitor and the pass element occurs at much lower frequency providing higher power supply ripple rejection. At heavy loads, the output impedance of the error amplifier and its open loop gain decreases, therefore reducing the PSRR between the DC and the unity gain frequency of the feedback loop. The voltage headroom or input to output differential, on the other hand, can also affect the PSRR performance. Decreasing the headroom decreases the overall gain of the error amplifier and this can be intensified with the effect of increasing the load current. At very low headroom, the LDO provides little power supply noise rejection [26]. This becomes worst at the drop-out region where the open loop gain of the error amplifier provides almost no power supply noise rejection as shown in Figure 2- 9.

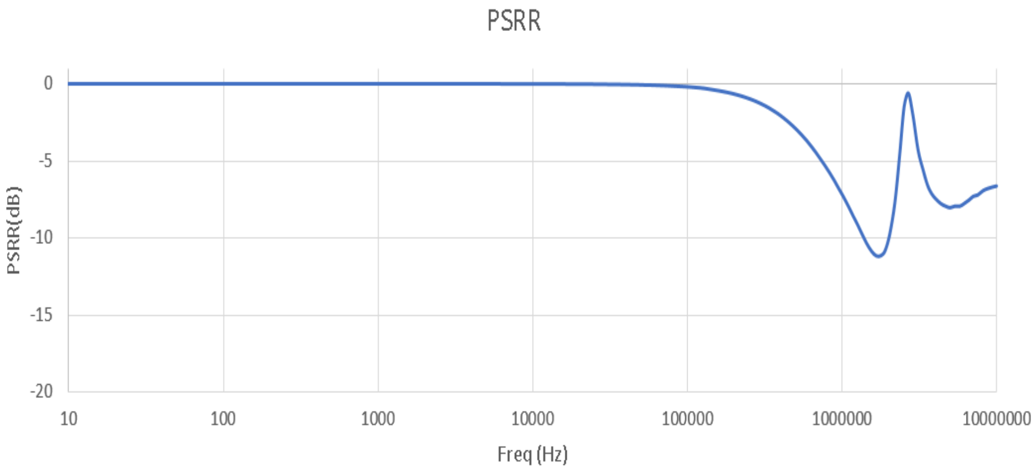

Figure 2- 9: LDO PSRR at drop-out region

LDO is quite useful as an active filter. However, headroom and load current must be carefully considered. Large voltage headroom is undesirable specifically at higher load current because it dissipates more power and therefore degrades the efficiency. This is a trade-off when system designers wish to improve the power supply ripple rejection through increasing the voltage headroom at the expense of lower efficiency. In addition, most LDO has unity gain bandwidth of less than 1 MHz and is not effective when filtering output ripple from switching regulators operating above 1 MHz switching frequency.

3

Novel Concept of an Auto-tune Resonant Filter with Variable Capacitor based Solution for Reducing Ripple in SMPS

An effective approach of using series resonance to significantly filter the fundamental ripple frequency is established. This is through the formation of a notch filter where it provides large attenuation on the discrete target frequency interferer. However due to component values, tolerances and part specifications drift, the challenge of aligning the fundamental ripple frequency and the resonant frequency becomes apparent. A novel auto-tuning phase detection circuit with a tunable based variable capacitor solution has been developed. This essentially controls and varies the notch filter frequency in alignment to the fundamental ripple frequency maximizing the ripple attenuation.

Figure 3- 1 shows the high-level block diagram of an auto-tuning resonant filter. The coupled inductor filter block in combination with the variable capacitor serves as the resonant filter circuit. A notch filter is formed on the coupled inductor filter block to effectively filter the fundamental ripple frequency coming from the SMPS. The phase detector detects the phase difference of the fundamental ripple signal passing through the input and output of the resonant filter. An error signal will be generated from the phase detector output in accordance to the phase difference of input and output signal of the coupled inductor filter. The error signal will be applied to the input of the tuning circuit. The tuning circuit is an integrator circuit which integrates the error signal and drives the variable capacitor to achieve a zero error signal voltage coming from the phase detector output [21]. By pushing the error signal to zero constitutes both input and output signal of the resonant filter is in phase achieving resonance within the close loop system therefore maximizing fundamental ripple attenuation.

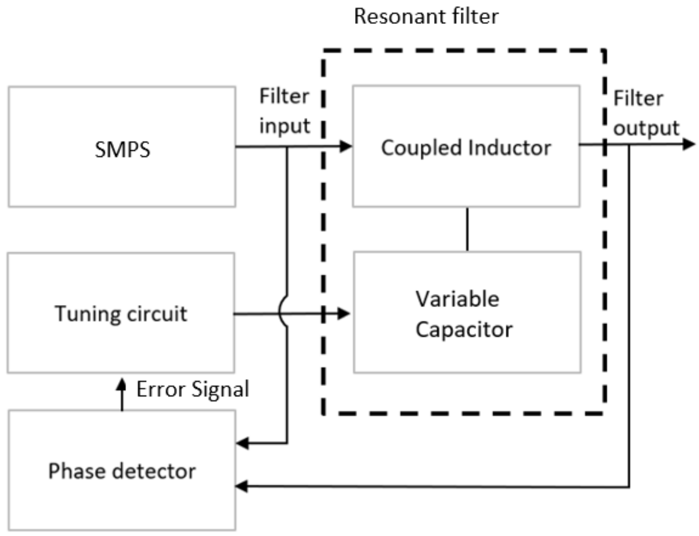

Figure 3- 1: High level block diagram of auto-tuning resonant filter

3.1 Resonance theory

Resonance is the result of perpetual oscillations in a circuit as stored energy is continuously passing between two reactive components, inductor and capacitor. Moreover, it occurs where both reactive component reactance that are 180 degrees out of phase are equivalent and cancels out. Therefore, the voltage and current are in phase and it is said to be purely resistive [27].

Resonance employs a frequency determined by the value of the capacitance and inductance. Equation (7) and (8) depicts the reactance of inductor and capacitor respectively where *L* is the inductance, *C* is the capacitance and *f* is the frequency:

$$Xl = 2\pi f L \tag{7}$$

$$Xc = \frac{1}{(2\pi f C)} \tag{8}$$

Equating both terms and finding the frequency (*f*) will yield equation (9) as the resonant frequency equation.

$$f = \frac{1}{\left(2\pi\sqrt{LC}\right)} \tag{9}$$

Series and parallel resonance are the two fundamental circuit configurations. Figure 3- 2 shows a series LC configuration where it employs an inductor and capacitor connected in series. LTspice® simulation tool was used to determine the impedance and phase vs.

frequency curve across the series resonant circuit. LTspice® is a high performance SPICE based computer simulator software produced by Analog Devices Inc.

An AC current source of 1A was used, therefore any voltage probed across the two reactive components equates the exact impedance value.

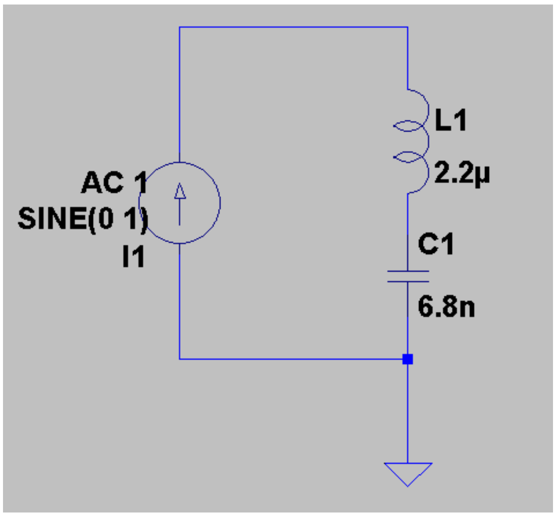

Figure 3- 2: Series LC configuration

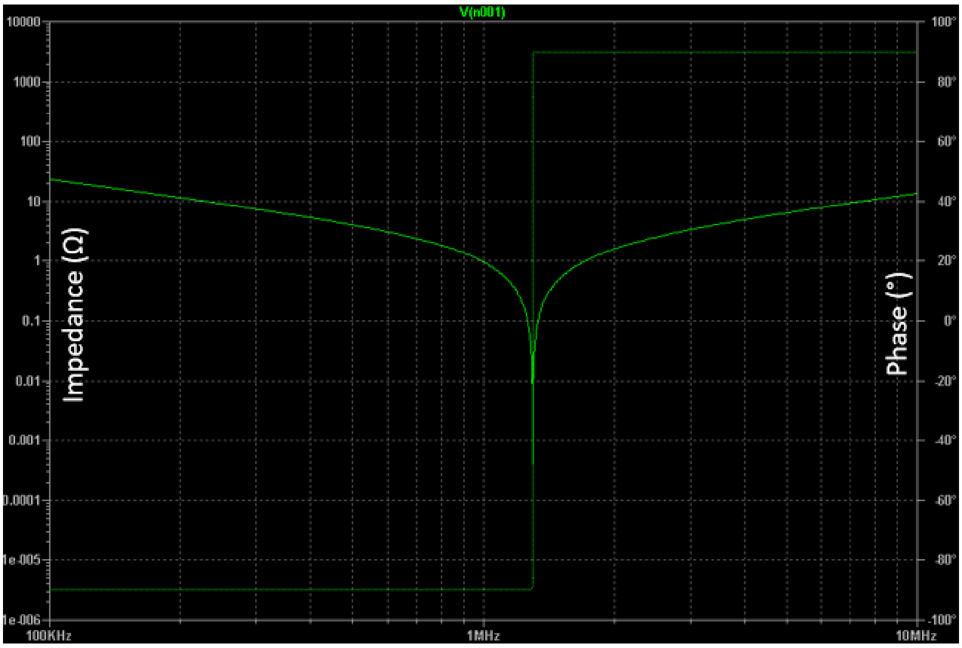

Figure 3- 3: Impedance and phase vs frequency curve simulation results for series LC configuration

Figure 3- 3 shows a sharp notch (band stop) at the resonant frequency of approximate 1.3 MHz. The bandwidth of the notch depends on the quality factor of the resonant circuit. Quality factor or Q factor is inversely proportional to the bandwidth [28]. It's a figure of

merit on how good the resonant circuit is. The higher the value, the narrower the bandwidth of the resonant circuit. A higher Q resonant circuit is desirable on filtering the fundamental frequency of the output ripple. The impedance before the resonant frequency is dominated by the capacitive reactance (negative phase) which has a decreasing impedance curve. Upon reaching the resonant frequency, both capacitive and inductive reactance cancels out and it is dominated by any series resistance in the circuit network. However, since only two reactive components are used in the simulation, the impedance of the notch frequency should be approaching zero. Else at resonance, the impedance is dictated by any resistive element in the circuit. After resonant frequency, inductive reactance dominates the overall impedance showing rising impedance curve (positive phase). The phase angle at resonant region shows a very steep change in phase from negative 90° to positive 90°. The steepness is highly dependent on the Q factor of the circuit. At resonance the phase angle is 0°.

Figure 3- 4 below shows a parallel LC or tank circuit configuration where it employs an inductor and capacitor connected in parallel. An AC current source of 1A was used, therefore any voltage probed across the two parallel reactive components equates the exact impedance value.

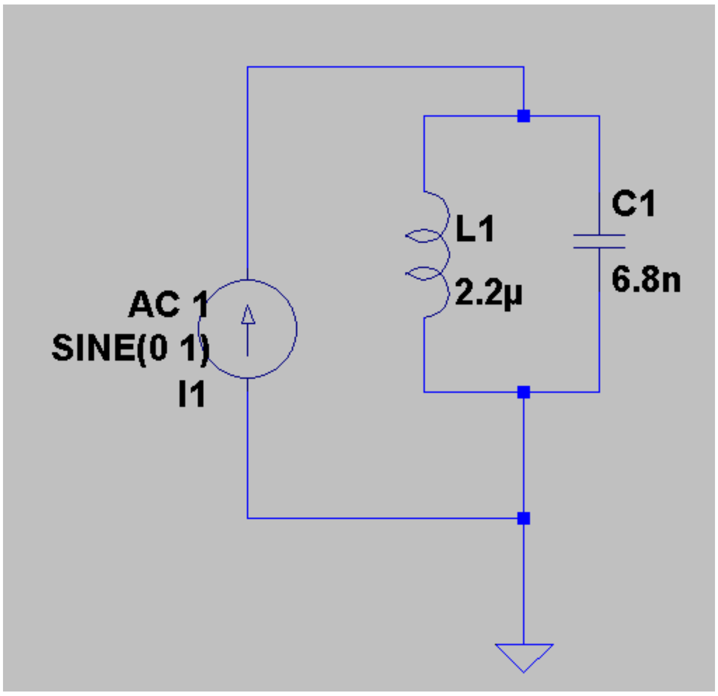

Figure 3- 4: Parallel LC configuration

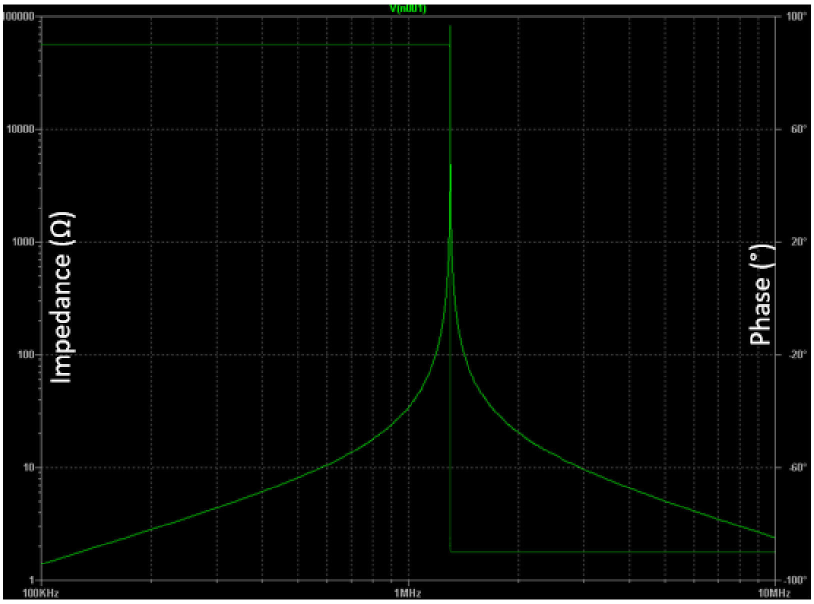

Figure 3- 5: Impedance and phase vs. frequency characteristics for parallel LC configuration

The results shows a sharp notch (bandpass) at the resonant frequency of approximate 1.3 MHz shown in Figure 3- 5 . The bandwidth of the notch filter depends on the quality factor of the circuit. The impedance before the notch frequency is dominated by the inductive reactance (positive phase) which has an increasing impedance. Upon reaching the resonant frequency, both capacitive and inductive reactance cancels out and it is dominated by any parallel resistance in the resonant circuit network. However, since only two reactive components are used in the simulation, the impedance of the resonant frequency should be approaching infinity. After resonant frequency, capacitive reactance dominates the overall impedance showing falling impedance curve (negative phase). It also shows a very steep change in phase from positive 90° to negative 90° at the resonance region due to very high Q.

3.2 The use of resonance as filter technique for power supply output ripple

A typical noise spectrum of most switching regulators comprises low frequency broadband noise or 1/f noise, fundamental output ripple and its harmonics. High frequency voltage ringing during switching transitions is translated as high frequency harmonics in frequency domain. Figure 3- 6 shows a typical noise output spectrum of a buck regulator.

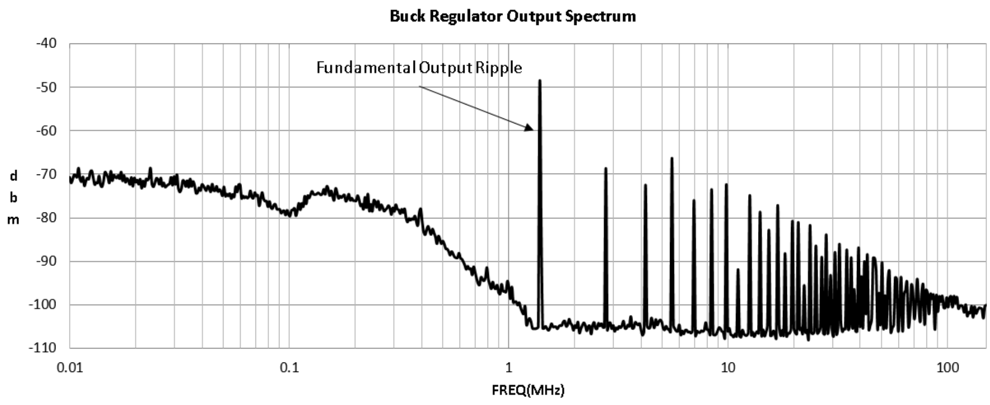

Figure 3- 6: Buck regulator output spectrum

From the plot, the highest noise amplitude is the fundamental output ripple. Its effects on some of the noise sensitive applications such as mixed signal processing converters were discussed in chapter 1. This should be significantly filtered or eliminated. The low frequency broadband noise can be mitigated by the inherent low frequency, high PSRR for most mixed signal processing converters while the high frequency noise (above 50 MHz range) can be filtered by high frequency passive filters such as ferrite beads.

A useful technique to significantly reduce the fundamental output ripple is using resonance. A high Q notch filter can be used to significantly attenuate the fundamental ripple as long it maintains the alignment between the fundamental ripple frequency and notch filter frequency. One example case is using a tank circuit. The tank circuit can be connected in series to the output of the switching regulator. The high impedance of the tank designed at the regulator’s switching frequency can significantly filter the fundamental ripple energy. Figure 3- 7 shows the results of having a tank circuit at the output of the switching regulator resonating at the fundamental ripple frequency.

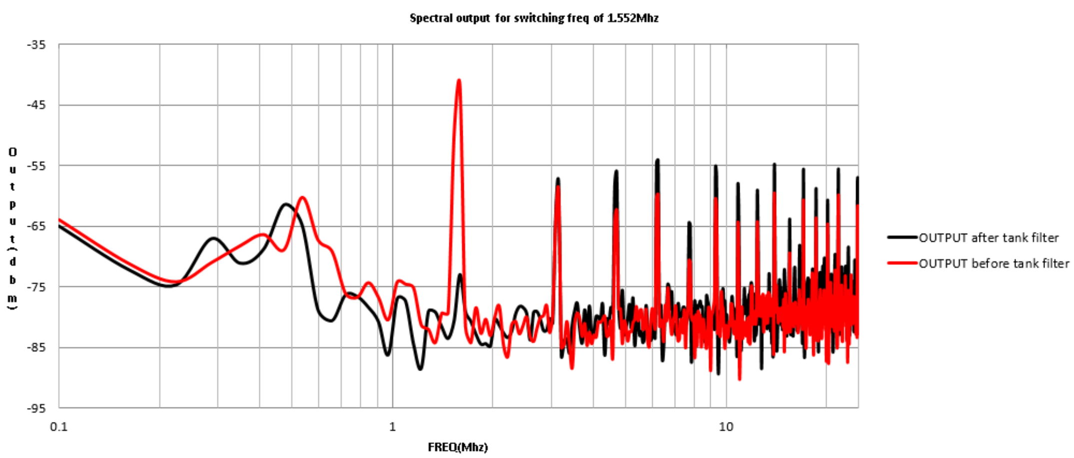

Figure 3- 7: Tank resonant filter effects on switching regulator output

From the results, the notch filter contributes more than 35dB of rejection and this rejection highly depends on the q factor of the resonant circuit. The harmonics are not considerably attenuated since the tank works as a band stop filter at resonant frequency. However, adding decoupling capacitors together with the tank circuit can further knock down the fundamental ripple frequency and its harmonics [29]. The same concept can be applied using a series resonance, utilizing its very low impedance characteristic. A series LC circuit can be shunted across the output of the switching regulator. This will provide a short to ground path for the AC currents at the resonant point.

3.3 LC coupled inductor filter concept

At least two inductors with a finite separation that affect each other by the means of magnetic field generated either one of them can be described as magnetically coupled. Transformer is an example of fundamental device comprises of separated coils that uses magnetic coupling between the primary and secondary coils to transfer energy from one circuit to another [30]. The coil can be depicted as an inductor. When two inductors are near to each other, a time varying magnetic flux caused by time varying current from one coil can link to the second coil. In effect, the time varying magnetic field or magnetic flux will induce a voltage across the second coil terminals. Therefore, this ability of having one inductor to induce a voltage across another inductor in proximity is called mutual inductance [31]. Mutual inductance can be written as:

$$M = k\sqrt{L1\ x\ L2} \tag{10}$$

Where *M* is the mutual inductance in henry, *k* is the coupling coefficient ranging from 0 to 1, *L1* and *L2* are the two-inductance placed in proximity.

Coupling coefficient is the fraction of magnetic flux produced by time varying current from one coil that links to the other coil. Its maximum value is one where the entire flux (100%) links to the other coil. Zero coupling coefficient value depicts no coupling between the two coils.

The coupled-magnetic filter concept was applied using coupled inductors. The use of coupled inductors in a two stage LC low pass filter can provide significant reduction on switching power supply output ripple. This is due through the formation of a notch filter that can be tuned near the exact frequency location of the output ripple. This provides adequate ripple attenuation using resonance in comparison with the conventional two stage LC low pass filter. Figure 3- 8 shows the schematic diagram of the coupled inductor in a two stage LC filter applied at the output of switching regulator.

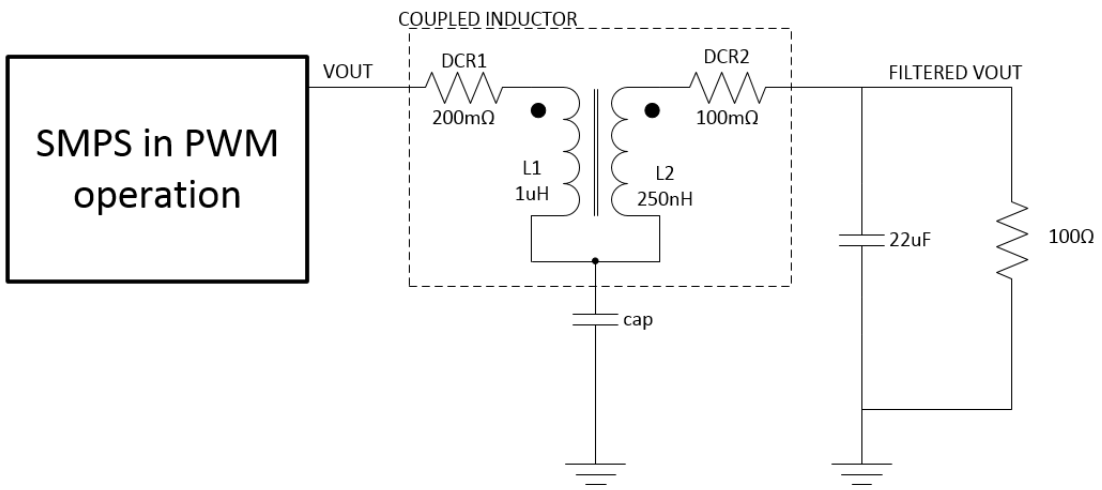

Figure 3- 8: Coupled inductor implemented in two stage LC low pass filter

The coupled inductor is set as 2:1 turns ratio (should be minimum of 1.5x turns ratio) with primary inductance of 1uH and secondary inductance of 250nH with both the inductors in series opposing to each other [32]. A series opposing configuration will produce an equivalent "T" model network of inductors as shown in Figure 3- 9 [33].

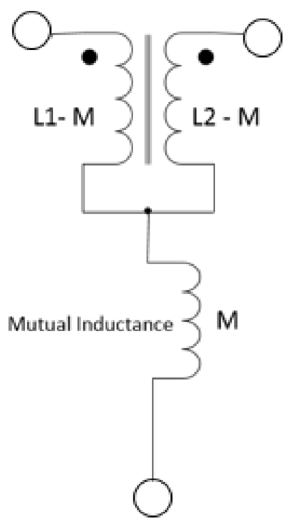

Figure 3- 9: Equivalent "T" model

Figure 3- 10 and Figure 3- 11 shows the circuit simulation (ADIsimPE powered by SIMetrix/SIMPLIS) and simulation results of the gain vs. frequency response (probed

across the 100Ω resistor) with coupling coefficient of 93% using two capacitor values: 30nF and 20nF respectively.

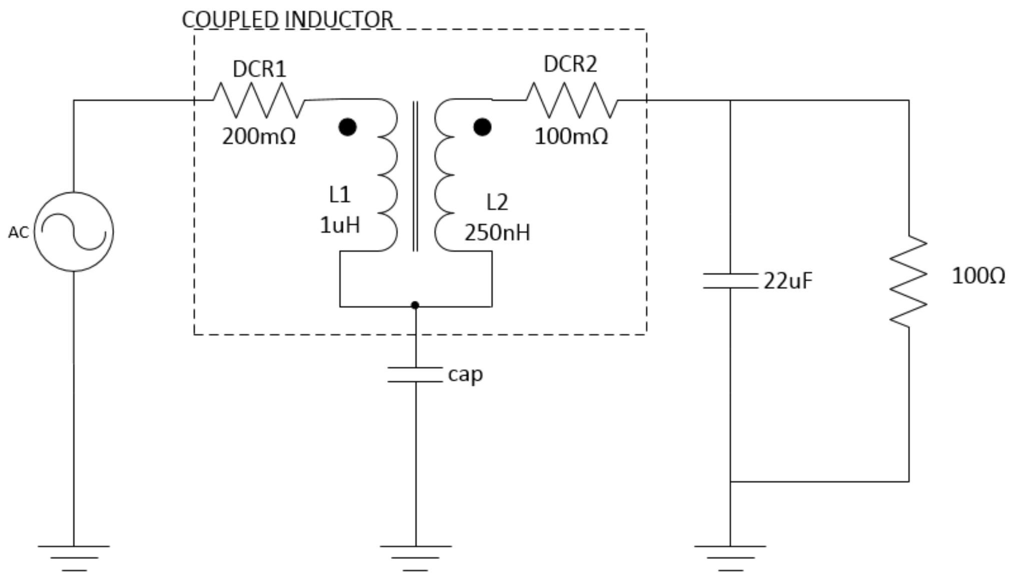

Figure 3- 10: Circuit simulation of coupled inductor implemented in a two stage LC low pass filter

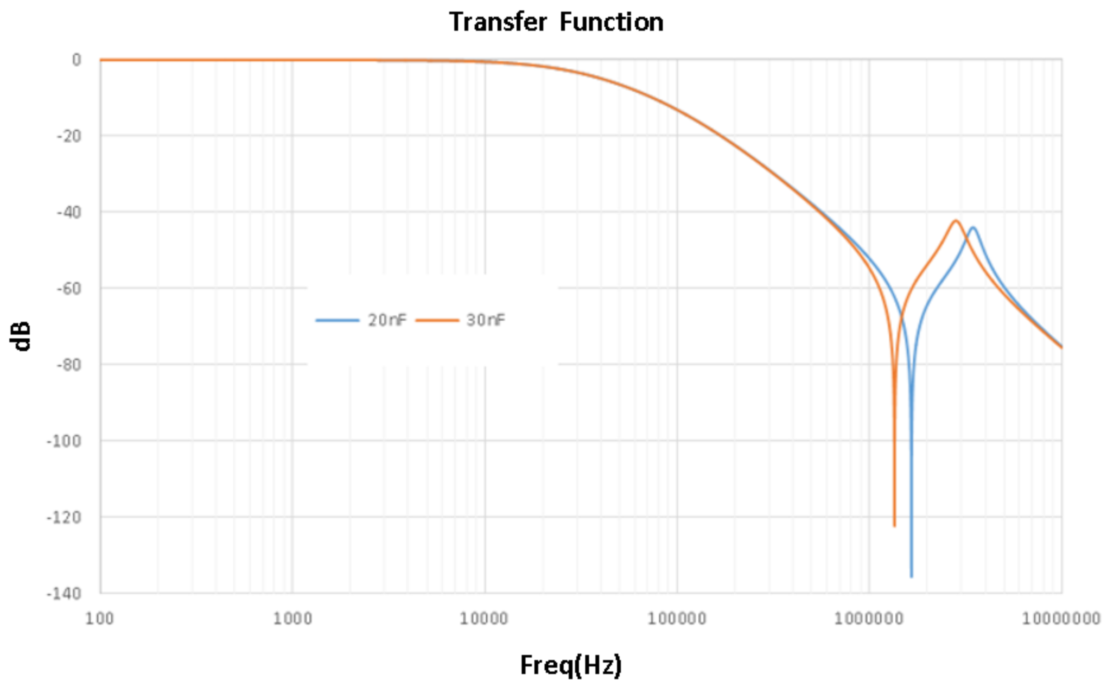

Figure 3- 11: Simulation results using two capacitance values

Figure 3- 11 describes that a notch frequency can be design and applied as power supply ripple filter. This is true as long the notch frequency aligns to the output ripple frequency.

3.3.1 Turns ratio

To generate an effective notch filter, a good turns ratio should be at least 1: 2. The proposed turns ratio was evaluated using LTspice® simulator. The turns ratio are interchangeable for both inductors and will yield the same notch filter frequency response. Figure 3- 12 shows the circuit simulation schematic with coupling coefficient of 0.93. The chosen value is within the same range (>0.9) of the off the shelf coupled inductor's coupling coefficient investigated in chapter 4 to simulate near actual performance. Mutual inductance is directly proportional to the coupling coefficient.

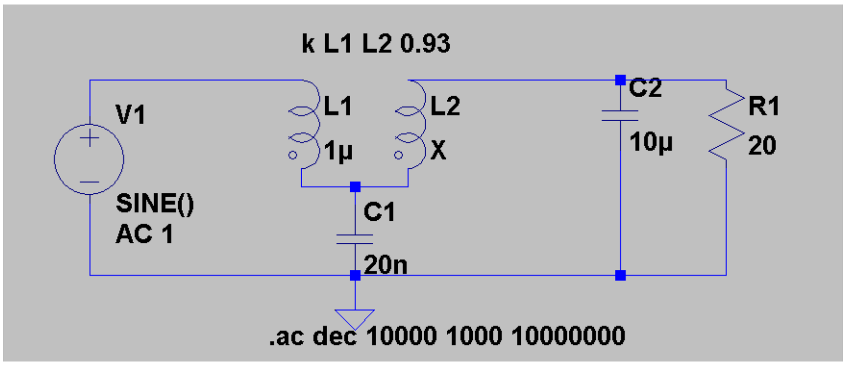

Figure 3- 12: Circuit simulation of varying coupled inductor turns ratio

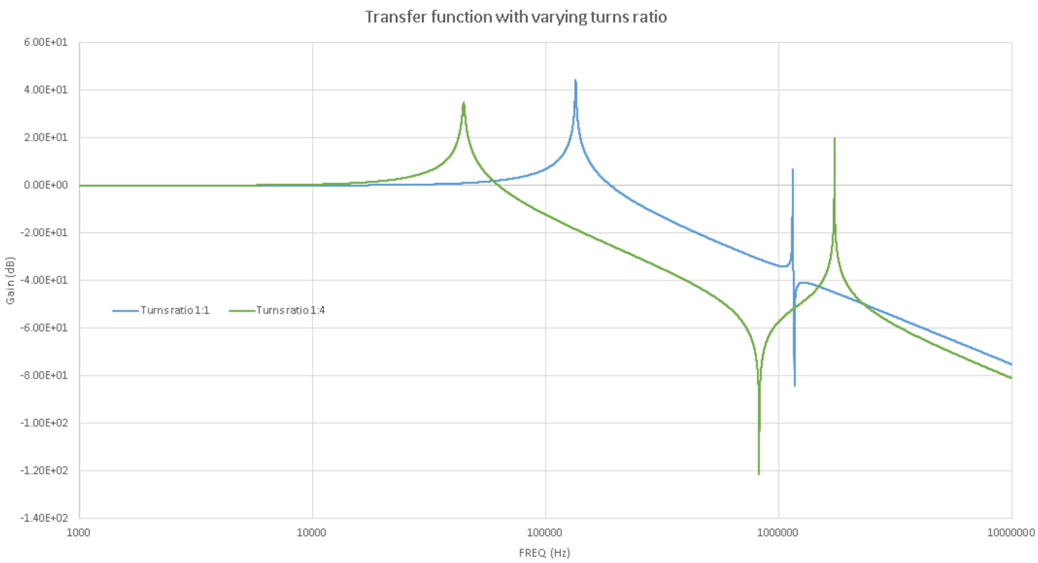

Figure 3- 13: Simulation results of varying coupled inductor turns ratio

It was seen from the plot that varying the secondary coil value (turns ratio) will produce changes on the notch frequency. Increasing the secondary coil inductance will also increase the mutual inductance thus the resonant frequency goes lower. Looking more closely on the notch frequency range as seen in Figure 3- 13 provides a usable notch filter at greater than times four of the inductance to the other linked inductor (turns ratio of 1:2).

However, it also resulted peaking at different frequency locations. This is due to the other resonance interaction of the inductor and capacitor in the circuit. This is detrimental because it negates the attenuation effect.

3.3.2 Effect of inductor's DC resistance and capacitor's equivalent series resistance

An inductor has an inherent small DC resistance associated with the coil windings. In principle, the amount of impedance for DC current is only dominated by DCR. Increasing the frequency also increases the overall impedance in a linear fashion at a point until other parasitic components take effect within an inductor. Parasitic stray capacitance due to capacitance for the intra-winding and capacitance between the winding and the core [34] will not be covered in this thesis. To demonstrate the DCR effects, a filter circuit having a component assumption value of 100mΩ and 200mΩ of DCR for both inductors with inductance of 1uH and 4uH respectively (see Figure 3- 14) was simulated using LTspice®. The simulation results shows that the undesired resonance peaking was reduced significantly (see Figure 3- 15). This is due to the series damping effect of the resistive element.

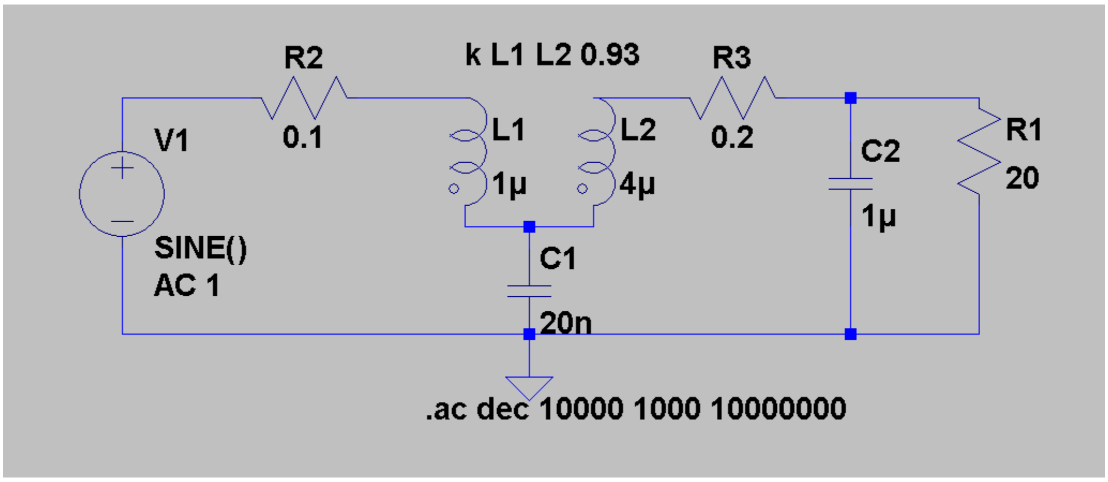

Figure 3- 14: Circuit simulation with added series damping resistance

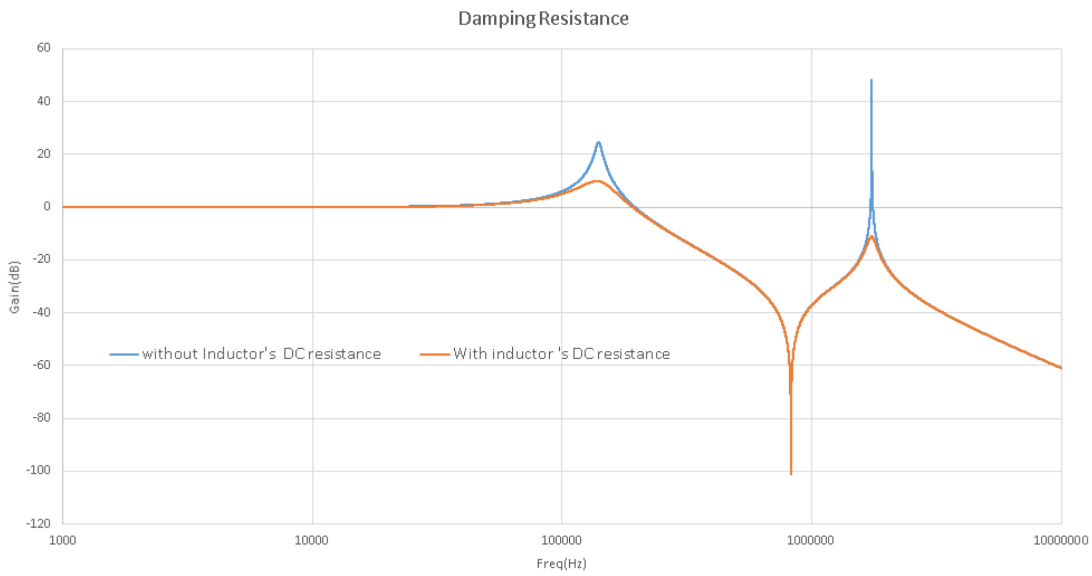

Figure 3- 15: Effects of series damping resistance

It can also be seen from the results that the notch filter depth of attenuation does not change. The series resistive elements only damp the undesired resonant peaks. However, the disadvantage is the added resistance along the rail that constitutes larger voltage drop and higher power dissipation specifically at higher load currents. Therefore, voltage accuracy at point of load will be affected.

Figure 3- 16 shows a small DC resistance connected in series to the shunt capacitor (C1).

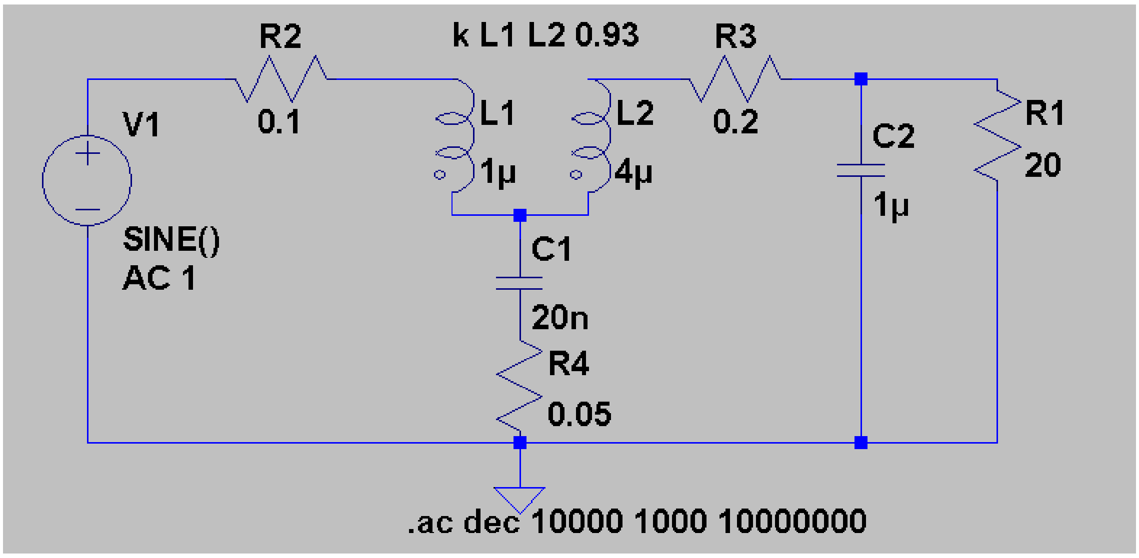

Figure 3- 16: Circuit simulator adding series resistance to middle capacitor (C1)

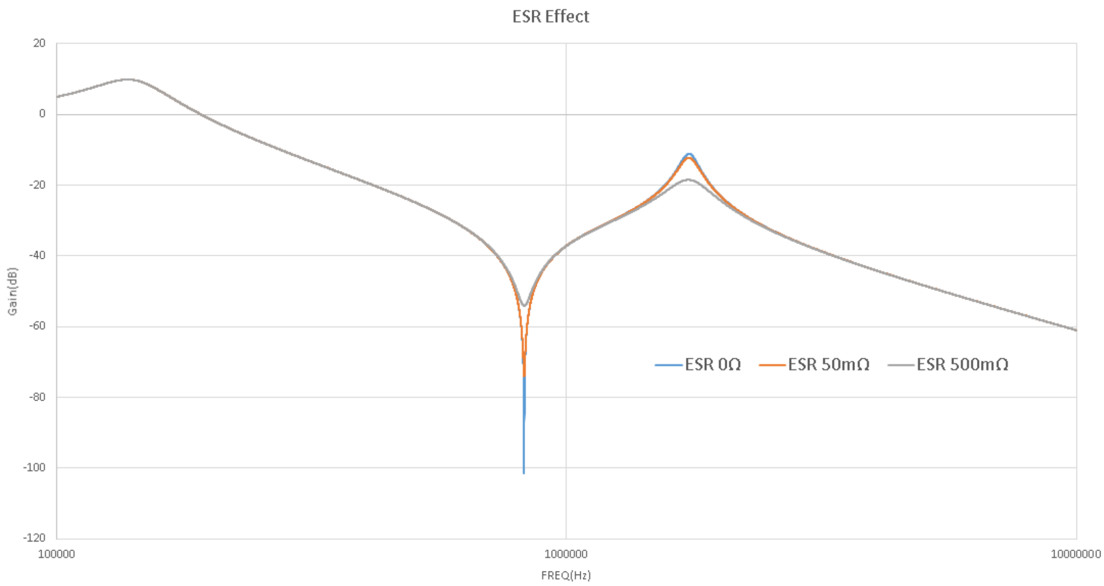

Figure 3- 17: Simulation results of adding series resistance to the middle capacitor

Figure 3- 17 shows that the attenuation depth of the notch filter decreases due to the added resistive loss on the shunt path. However, the second resonant peak also shows noticeable reduction as well. Shunt capacitor's ESR should also be considered when designing the effective notch filter. The preferred ESR should be low to further enhance the attenuation depth of the notch filter if fundamental output ripple is a concern.

3.4 BST or multi-layer ceramic capacitor as variable capacitor

To provide the required tuneability of resonant frequency in relation to the switching frequency of the SMPS, variable reactive component as a tuning element is considered. In this research, variable capacitors such as BST (Barium Strontium Titanate) dielectric and ceramic capacitors were considered due to its immediate availability and wide capacitance tuning range, as the variable resonant component.

The use of variable capacitor can provide novelty for the use of switching power supply filtering. One application is the use of tuneable notch filter. This is achieved by generating various resonance using variable capacitance with fixed inductor element. Depending on the configuration and how it was implemented, maximum impedance (parallel LC) and minimum impedance (series LC) can be accomplished if the notch filter frequency aligns to the target frequency interferer.

Three possible variable capacitor tuning configurations are shown Figure 3- 18.

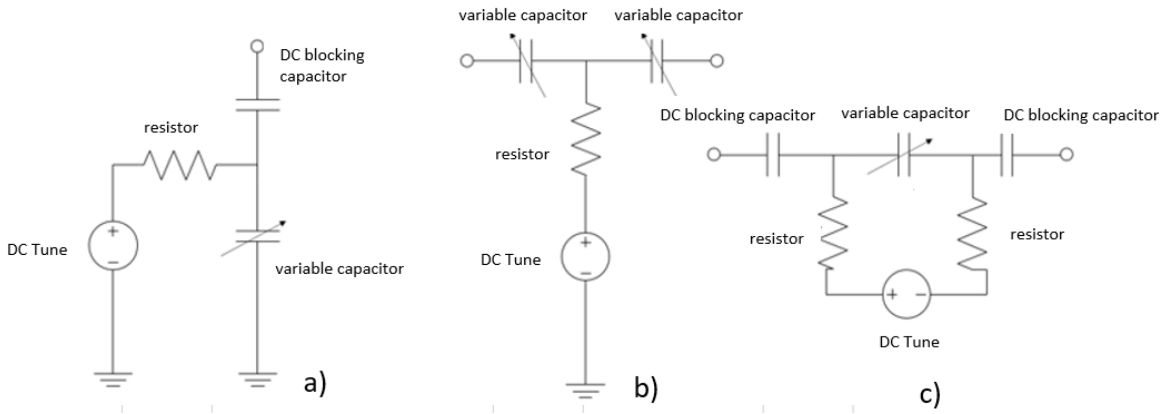

Figure 3- 18: Various variable capacitor tuning configuration

The DC tune is the tuning voltage to vary the capacitance value. The variable capacitor filter network should have an isolation to the DC tune which can be implemented by adding a series resistor. In addition, the DC tune should also not interfere to the AC signal to be filtered or to the rest of the circuity. This is achieved by using a DC blocking capacitor (can be a fixed value capacitor).

3.4.1 Barium Strontium Titanate dielectric

Barium Strontium Titanate or BST capacitor is tuneable capacitor wherein its capacitance can be varied by applying voltage across it. The dielectric (BST) exhibits a change in molecular structure once a varying DC voltage is applied. The polarization varies with the applied voltage then consequently changes the dielectric constant and therefore the capacitance [21].

3.4.2 Behavioural response of the BST capacitor as function of DC tuning

A BST IC die is internally fabricated in ADI using two series BST capacitors packaged in a SOIC package (further discussion and sample photos is seen in chapter 4). Figure 3-19 shows the DC tuning configuration used in characterizing the actual BST capacitance change response. A LCR bench type meter is used to accurately measure the capacitance across p and n terminals. The Vc voltage or DC tune is an external bias which is varied from -7V to 7V. A series resistor (10kΩ) is used after the DC input to provide adequate impedance isolation and the test frequency of the LCR bench equipment is 100 kHz.

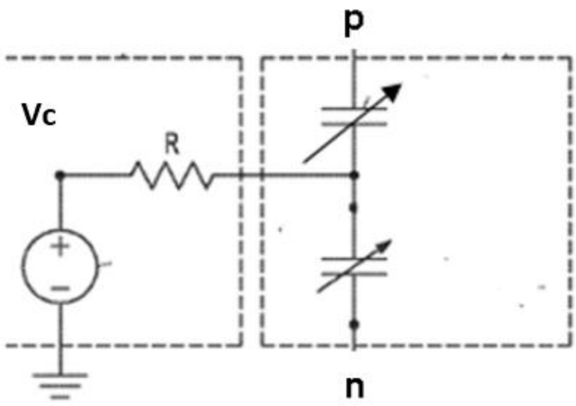

Figure 3- 19: Actual tuning configuration

Figure 3- 20 shows the actual measurement results. The total series capacitance for 0V DC is around 9nF. Both positive and negative DC input yields near symmetrical response. At +/-7V, the actual total capacitance is approximately 3.9nF. Thus, the BST capacitor is a good variable capacitor candidate that can produce a tuning ratio of at least 1:2.

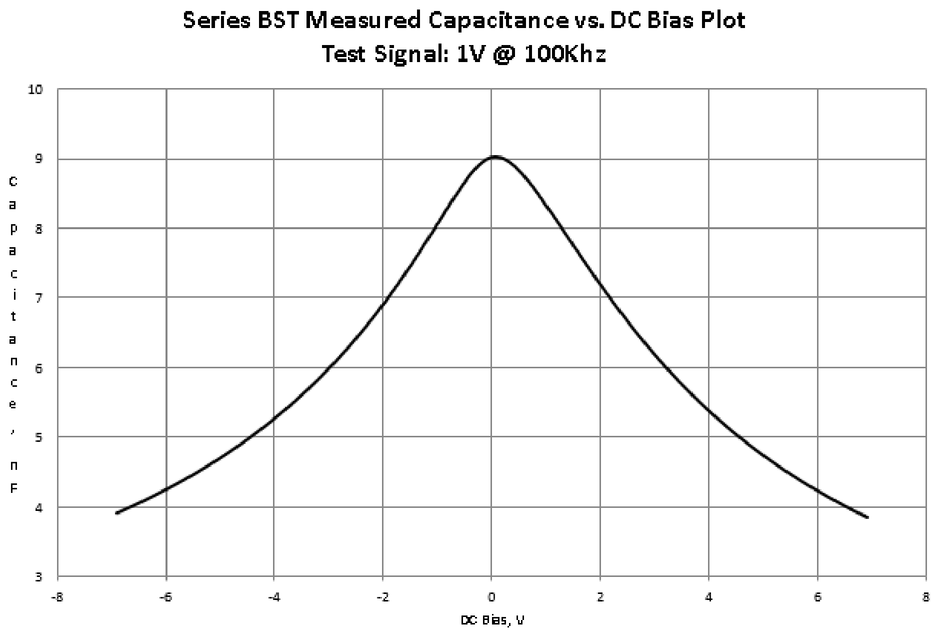

Figure 3- 20: Measured capacitance across DC bias

3.4.3 Behavioural modelling of BST capacitor using Verilog-a

This section provides a behavioural model of BST dielectric capacitor using Verilog-a. A 6th order polynomial trend line (red dashed) is first curve fitted to the measured plot as shown in Figure 3- 21.

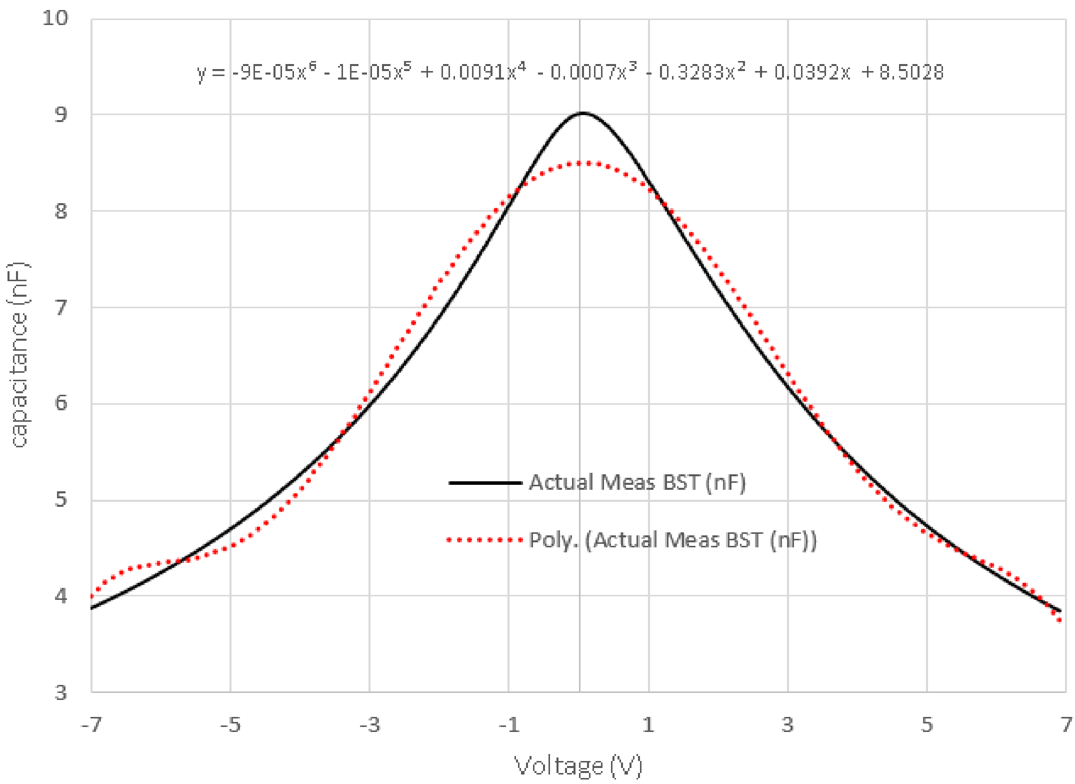

Figure 3- 21: Actual measurement vs. trend line

The capacitance equation as function of DC voltage yields:

$$C(nF) = -0.00009Vc^6 - 0.00001Vc^5 + 0.0091Vc^4 - 0.0007Vc^3 - 0.3283Vc^2 + 0.0392Vc + 8.5028 \quad (11)$$

Where:

- *Vc* is the DC tuning voltage or the control voltage
- *C* is the capacitance

This suggest that the 6th order polynomial trend line is quite close at some points to the actual measurements but there are points which have larger error approximately around 5~6 %. A percent error of less 6% can still be acceptable to generate a near model approximation of the BST.

A three terminal capacitor is built in Verilog-a consisting of p, n and Vc terminals (Figure 3- 22). The terminal p and n are the terminal nodes across the two series BST capacitors including the series ESR and ESL. The Vc terminal is the control voltage.

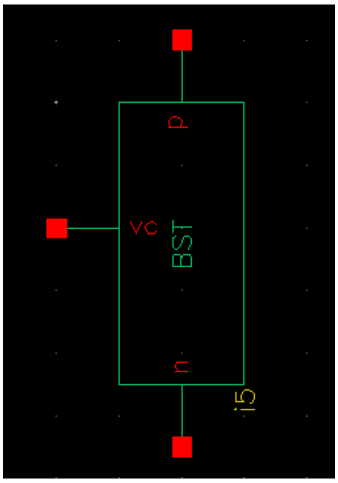

Figure 3- 22: BST Verilog-a model using Cadence Virtuoso

The control voltage Vc is declared as input terminal while the p and n terminal is declared as both input and output terminals. All BST terminal nodes are electrical in nature.

The trend line polynomial equation is used for the BST behavioural model. The equation is implemented in Verilog-a text editor.

$$\mathrm{C} = \left(\mathrm{p0} + \mathrm{p1} * \mathrm{pow}(\mathrm{Vd}, 1) + \mathrm{p2} * \mathrm{pow}(\mathrm{Vd}, 2) + \mathrm{p3} * \mathrm{pow}(\mathrm{Vd}, 3) + \mathrm{p4} * \mathrm{pow}(\mathrm{Vd}, 4) + \mathrm{p5} * \mathrm{pow}(\mathrm{Vd}, 5) + \mathrm{p6} * \mathrm{pow}(\mathrm{Vd}, 6)\right) * 0.000000001 \tag{12}$$

The coefficients p0 to p6 are the coefficient of the trend line, in which are declared as parameters with values specified. Vd is defined as the voltage in Vc.

The BST is approximated with an inclusion of series parasitic elements which are resistor (ESR) and inductor (ESL). ESR is set at 0.003Ω to easily determine the resonant point for a deeper notch and ESL is set at 900ph to provide high resonant frequency point. These will later be used in the capacitance calculation across sampled control voltage. The contribution statement under the analog process describing the relationship between the signal's yields:

$$\mathrm{V}(\mathrm{p}, \mathrm{n}) < +\mathrm{r} * \mathrm{I}(\mathrm{p}, \mathrm{n}) + \mathrm{l} * \mathrm{ddt}\big(\mathrm{I}(\mathrm{p}, \mathrm{n})\big) + \frac{\mathrm{idt}\big(\mathrm{I}(\mathrm{p}, \mathrm{n})\big)}{\mathrm{c}}; \tag{13}$$

Resistor voltage is defined as the product of parameter resistance (r) and the current branch between the p and n terminals. Inductor voltage is defined as the product parameter inductance (l) and the time derivative of the current branch between p and n terminals. The capacitor voltage is the quotient of the time integral of the current branch between p and n terminals and the capacitance c.

Therefore, the voltage between the p and n terminal is bounded by the summation of the voltages of the capacitor, resistor and inductor.

An ADICE simulator (ADI proprietary simulation tool) is used to test the Verilog-a behavioural model of the BST. In order to validate the model, the impedance vs. frequency plot is acquired. This is accomplished by having an AC current source in parallel with BST. A 100GΩ is placed in parallel across the BST to provide DC path while avoiding compilation errors (initial condition is open circuit). The sample test bench schematic can be seen in Figure 3- 23. The current source is set to 1A. The parallel resistor has resistance that is significantly larger than the impedance of the BST. A DC supply generates the Vc voltage for the BST to vary the capacitance. Thus, the measured voltage across terminal p and n is the equivalent impedance value of the BST.

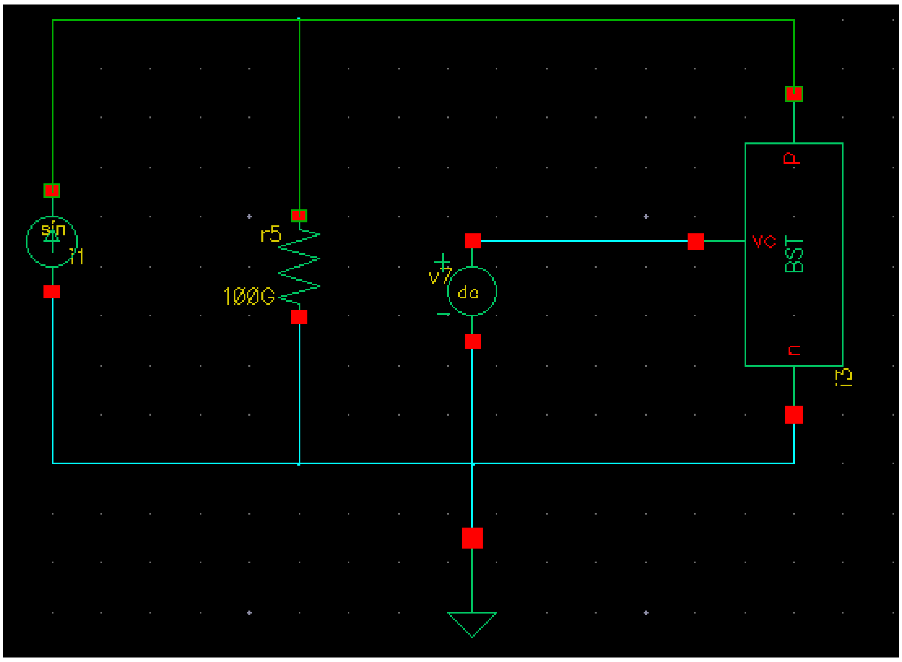

Figure 3- 23: Test simulation bench circuit

Figure 3- 24 shows the impedance vs. frequency simulated plot for DC tuning of 0V, 3.5V and 7V. The capacitive curve region has increasing impedance with decreasing capacitance which is expected. The self-resonance of the BST for the 0V, 3.5V and 7V vc are around 57.5 MHz, 69.08 MHz and 87.17 MHz respectively (decreasing capacitance while inductance is held constant increases self-resonance). Above self-resonance, the ESL dominates which shows increasing impedance with increasing frequency.

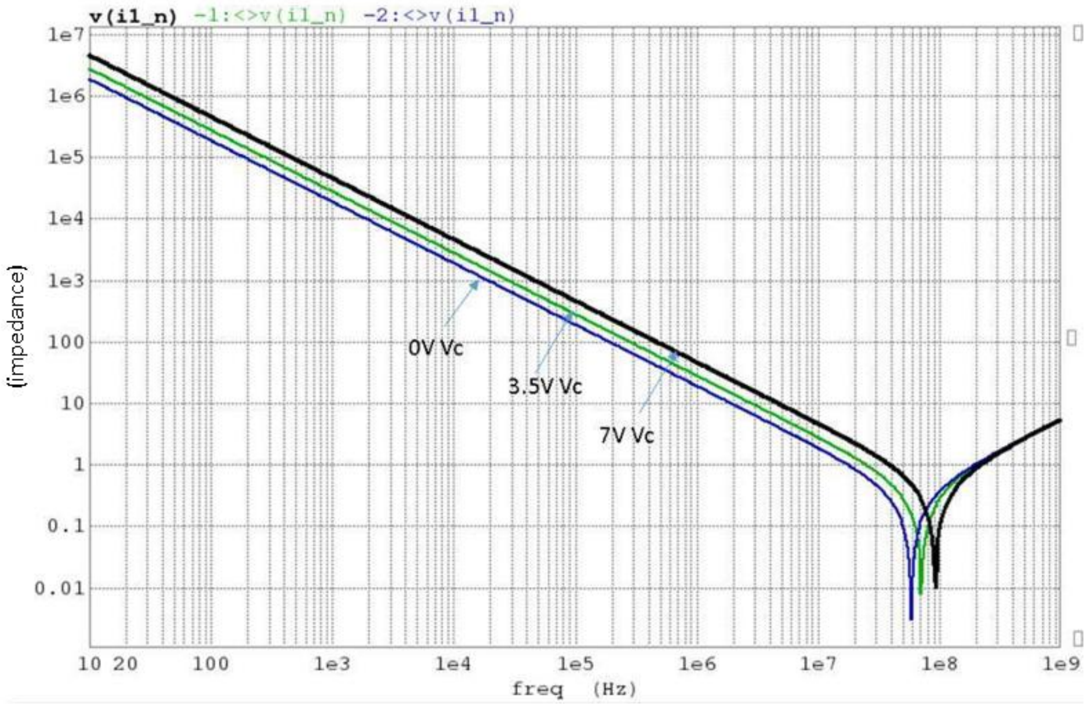

Figure 3- 24: Impedance vs. frequency curve

Figure 3- 25 shows the capacitance across DC tuning voltages acquired from the simulation results. This is compared with the trend line response. The dashed red curve is the trend line while the dotted points are the capacitance acquired from the simulation results for -7V, -3.5V, 0V, 3.5V and 7V Vc. This is calculated through the self-resonance equation with inductance held constant. The simulation results correlates with the trend line indicating successful implementation of the BST Verilog-a model.

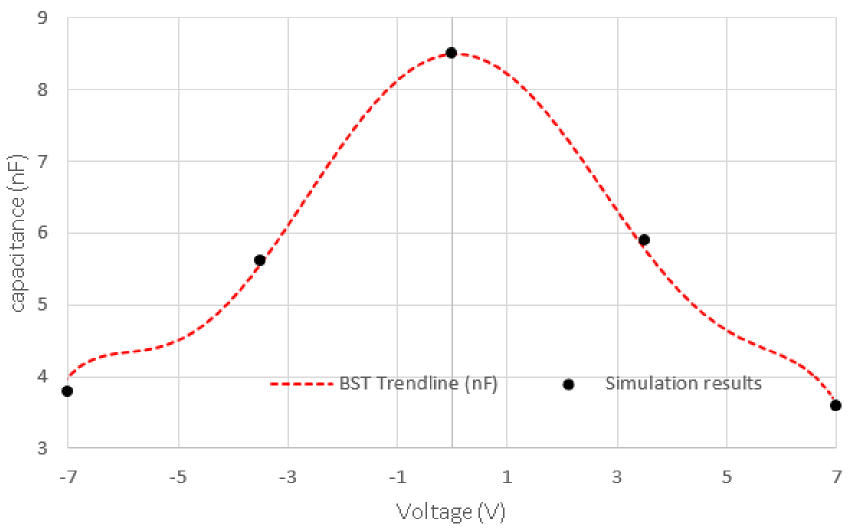

Figure 3- 25: Trend line vs. simulation

3.4.4 Multi-layer ceramic capacitor

MLCC or multi-layer ceramic capacitors are often used as decoupling capacitors. Implementing decoupling capacitors along the IC power supply bus mitigates the conducted ripple and noise on that path. It breaks the coupling between the circuit's portions making noise to travel through the capacitor (lower impedance) to ground path. MLCC ranges from pF to µF range of capacitance, have high voltage rating and low ESR. MLCC can be modelled as a simple series network of resistor (ESR), inductor (ESL) and capacitor(C) components, as shown in Figure 3- 26 [35].

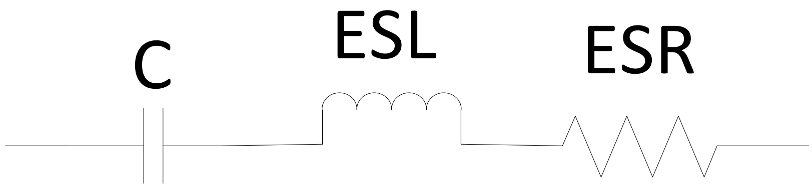

Figure 3- 26: Equivalent capacitor circuit model

The two general strays parasitic are ESL, effective series inductance and ESR, effective series resistance which depends on leads, dielectric type and structure of the capacitor. Ways of mounting the capacitor on the PCB also influences the values of these strays, i.e. long traces that connect the capacitor to the power supply line or ground increases ESR and ESL. These parasitic strays are frequency dependent and must be accounted for noise decoupling applications.

An ideal capacitor basically has decreasing impedance with increasing frequency. This is desirable since decoupling capacitor should effectively provide a low impedance path for AC signal on the IC supply line to ground. However due to parasitic strays, there will be negated effects. The series RLC model of the capacitor will have a frequency point where the reactance of the inductor (*ESL*) and the capacitor (*C*) will be equal. This is the self-resonant frequency of the capacitor and the total impedance will be limited to the resistive value(R). At high frequency region, the inductor (ESL) will dominate and will increase the impedance of the capacitor. These parasitic are important to consider especially for wide bandwidth decoupling, as what frequency will give the most signal attenuation.

The self-resonance(*fres*) yields the following equation:

$$fres = \frac{1}{\left(2\pi\sqrt{ESL\ x\ C}\right)} \tag{14}$$

An impedance vs. frequency curve of a MLCC is depicted on Figure 3- 27. The plot was acquired through using Murata SimSurfing design tool. It shows the capacitance dominates the impedance (blue) up to a self-resonance point. The overall impedance is now equivalent to the ESR (G) of the capacitor. Above resonance the ESL impedance dominates. It was seen most of the ceramic capacitor has high Q self-resonance due to its very low ESR.

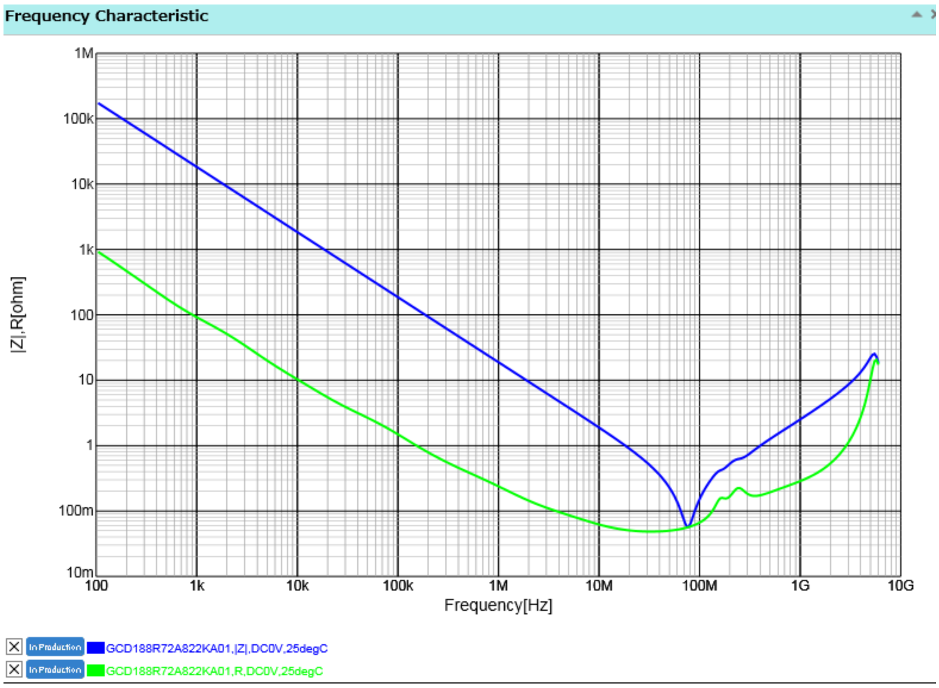

Figure 3- 27: Impedance and ESR vs. frequency curve (Murata SimSurfing tool)

Furthermore, a key characteristic of MLCC as a variable capacitance is to utilize its DC bias characteristics or the change in capacitance when a DC voltage is applied across the capacitor terminals. Capacitance, package size, temperature characteristic and voltage ratings are some of the key elements that influence DC bias characteristics. DC bias characteristics can be referred from the typical performance in the datasheet. Therefore, careful selection of MLCC for design-in as variable capacitance should be considered.

Figure 3- 28 shows the capacitance change of a 47000pF , 50V MLCC with varying package size.

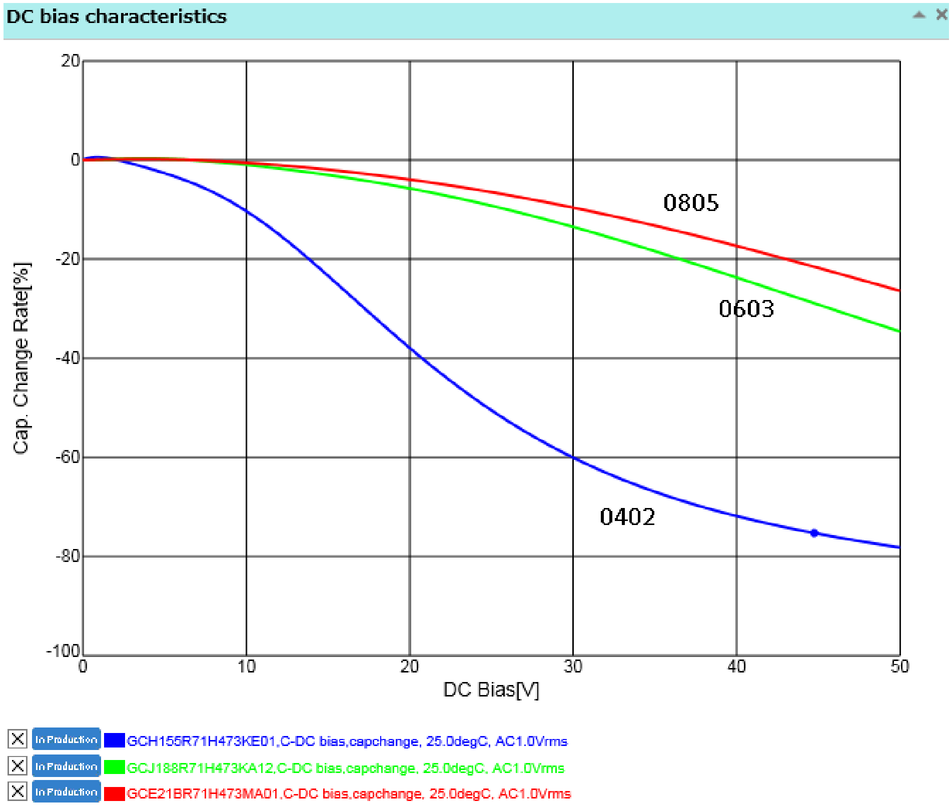

Figure 3- 28: DC bias vs capacitance change (Murata SimSurfing tool)

Notice with the same capacitance and voltage rating, package affects the capacitance change with respect to DC bias. The smallest package provides the largest change of capacitance compared to larger package. From 0V to 50V voltage rating can provide up to 80% capacitance change. Hence it shows that the wide capacitance change dependency with the DC bias can be useful for tuneability. Voltage rating can be carefully chosen from various MLCC such as to design the maximum voltage swing of the tuning circuit.

3.5 Auto-tune concept

3.5.1 Phase detection

Figure 3- 29 illustrates a high level design of switching power supply system including an auto-tuned power supply filter. The auto-tuned power supply filter circuit includes a first filter stage and a second filter stage. The first filter stage includes coupled inductor and a variable capacitor. The second filter stage is a shunted output capacitor.

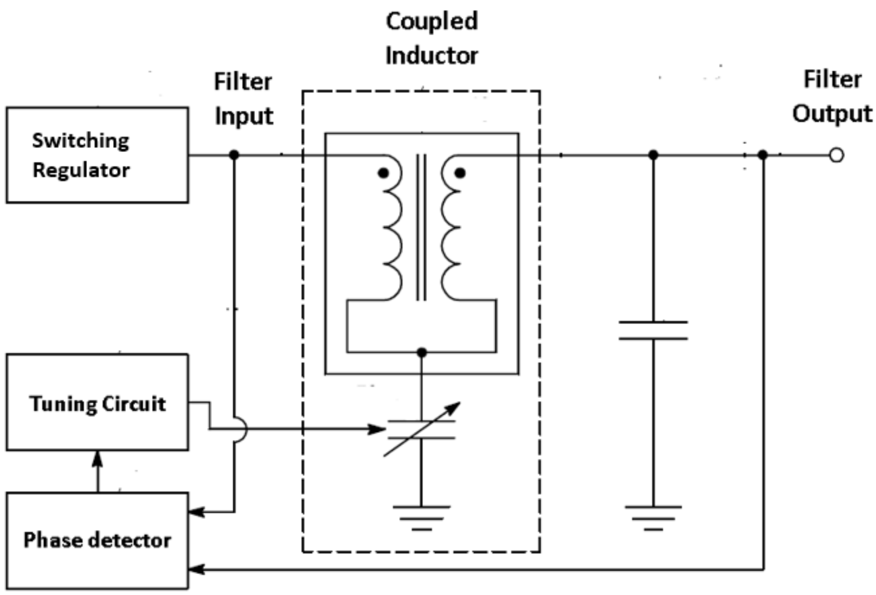

Figure 3- 29: High level design of auto-tune coupled-magnetic filter

The auto-tuned power supply filter includes a phase detector circuit. The amplitude and phase information of the input filter and output filter signals are detected. The phase detector circuit includes an analog multiplier to provide a zero average output or a zero error voltage to the tuning circuit with a 90° phase shift between the first and second inputs of the phase detector circuit. The 90° phase shift offset is due to the output capacitor at the second filter stage. Likewise, the phase shift of the coupled inductor and variable capacitor at the first filter stage is 0° due to resonance. This is to facilitate the alignment of the resonant notch to the fundamental ripple frequency of the switching power supply. See Figure 3- 30 for the bode plot.

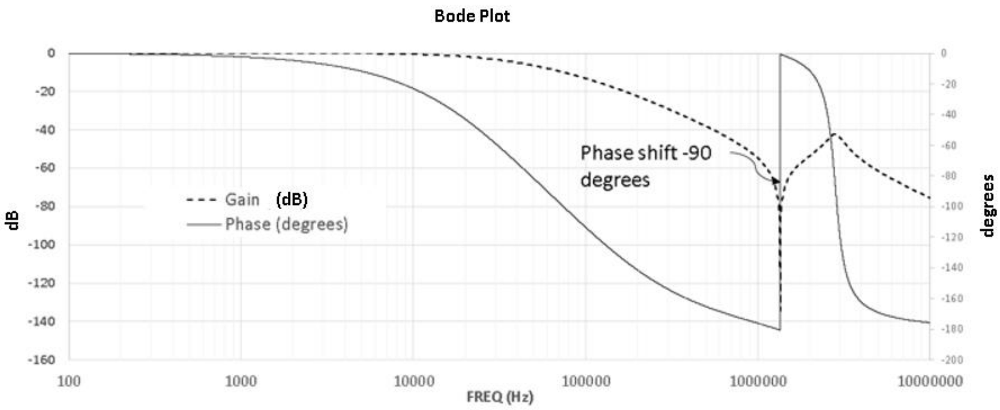

Figure 3- 30: Gain and Phase plot

The tuning circuit output is coupled to a tuning port of the variable capacitor. The tuning port is illustrated in detail in Figure 3- 31.

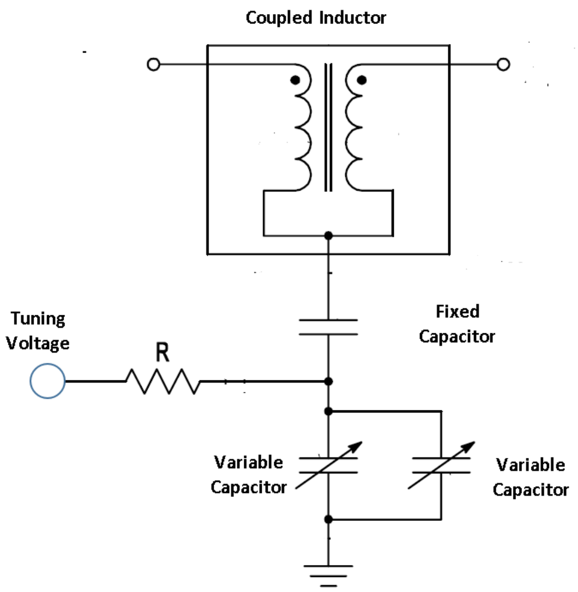

Figure 3- 31: Tuning port circuit

A fixed value capacitor having a first terminal coupled with the non-dotted terminals of the coupled inductor and a second terminal coupled with a first terminal of two variable capacitors connected in parallel between the fixed value capacitor and ground. The configuration should have an AC isolation to the tuning voltage which can be implemented by adding a series resistor. In addition, the tuning voltage should also not interfere the AC signal to be filtered or to the rest of the circuity. This is achieved by using a DC blocking capacitor which is the fixed capacitor. The two variable capacitors are connected in parallel configuration to achieve higher capacitance value.

The tuning circuit will generate the tuning voltage in accordance to the measured phase difference between the filter input and filter output signals. The capacitance value of the variable capacitor may be varied by varying the tuning DC voltage automatically according to system measurements or feedback loop. This align the resonant notch region of the frequency response of the auto-tuned coupled-magnetic filter circuit with the fundamental ripple frequency of the switching power supply. The phase difference information signal output from the phase detector circuit to the tuning circuit may control a DC tuning voltage applied to the variable capacitor via the variable capacitance tuning voltage port.

3.5.2 Integrator as a tuning circuit for driving variable capacitor

The integrator integrates the error coming from the analog multiplier output. The integrator drives the variable capacitor and corrects the feedback loop pushing the analog multiplier outputs to zero error voltage.

The rate of change in voltage due to the feedback capacitance depends on the charging current. Once the integrator corrects the loop and error voltage is being reduced, the charging current decreases and so is the rate of voltage change (dv/dt), until such time the rate is very small. This is said that the input signal frequency locks to the specified resonant frequency. A sample integrator simulation is depicted below using ADISimPE, a circuit simulator tool powered by SIMetrix/SIMPLIS.

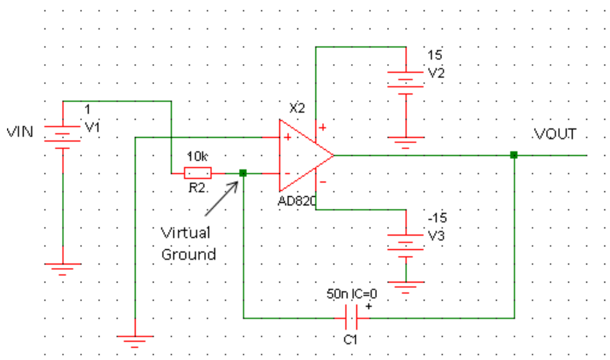

Figure 3- 32: Integrator circuit

The op amp operates a negative feedback operation in which the node after the 10kΩ become a virtual ground (inverting input). The non-inverting input is grounded for simplicity.

In that case a current (with V1 potential) which is constant flows through the 10kΩ resistor to the feedback capacitor. Note that the constant charging current (i) approximates to:

$$i = \frac{V1}{R2} = \frac{1}{10k\Omega} \tag{14}$$

Charging current is 100uA, while the node after 10kΩ is held at virtual ground.

Since the charging current is constant then we can use the capacitance equation(15):

$$i = c * \frac{dv}{dt} \tag{15}$$

The current i is 100uA, the capacitance is 50nF; the calculated rate of change of voltage with respect to time is 2kV/s in accordance with equation (16).

$$\frac{i}{c} = \frac{dv}{dt} \tag{16}$$

The rate of voltage change with respect to time can be seen on the output of the integrator. Therefore, in this case, a negative dv/dt or voltage rate-of-change in the output of the integrator yields as the constant current charges the capacitor. The polarity of dv/dt depends on the direction of the charging current. The input voltage is connected to the inverting input terminal of the op-amp thus a polarity reversal resulted in this manner.

The output voltage magnitude depends on the length of time the input voltage is present. The rate of change depends on the R, the C and the input voltage (charging current) as seen on the equation above. The gain is dependent on the reactance of the capacitor(Xc) over the input resistor ($R2$).

$$G = -\left(\frac{Xc}{R2}\right) \tag{17}$$

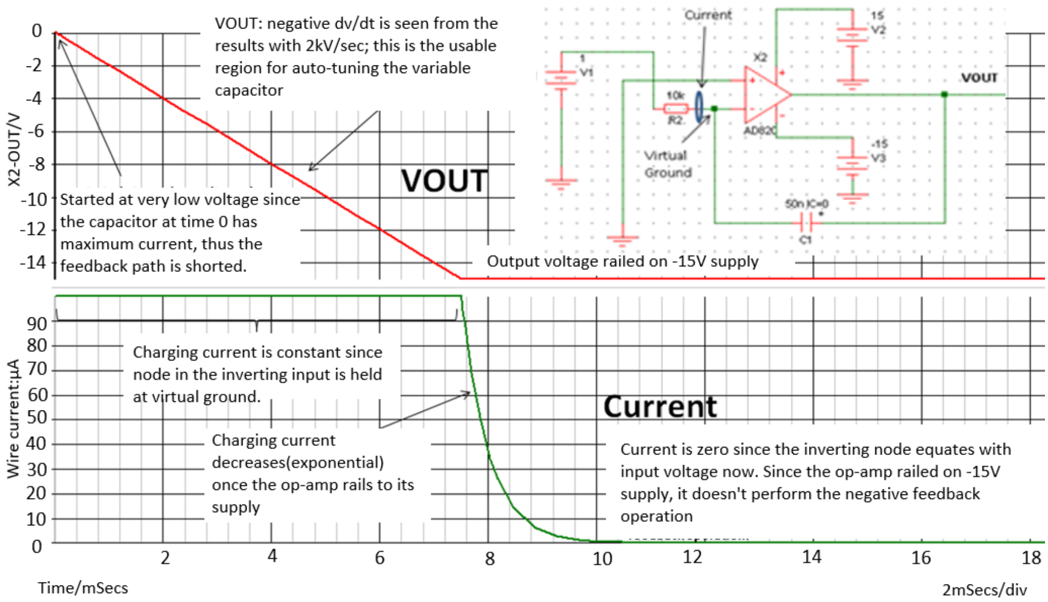

Figure 3- 33: Simulation results

With dv/dt = 2000V/sec, we can that for a 15V supply rail of the op-amp, the time it will rail to its supply is about:

1sec/2000V*15V = 7.5msec which can be seen on the simulation results in Figure 3- 33.

Below simulation is the comparison of VOUT vs. the inverting input voltage node

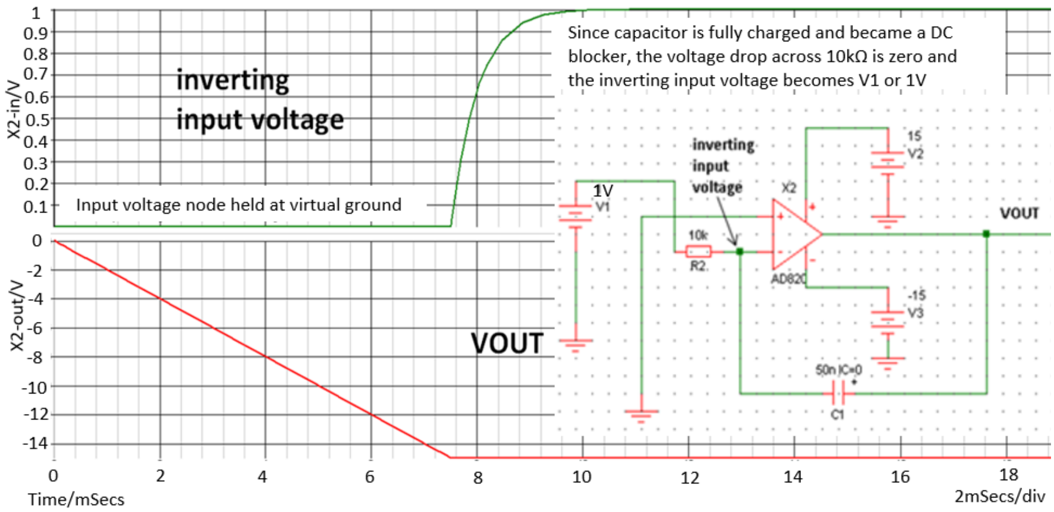

Figure 3- 34: Vout vs. inverting input voltage

Changing input voltage (while retaining R and C) changes the rate of change as shown in Figure 3- 35. The charging current was also plotted. Note that R and C should also affect the rate of change:

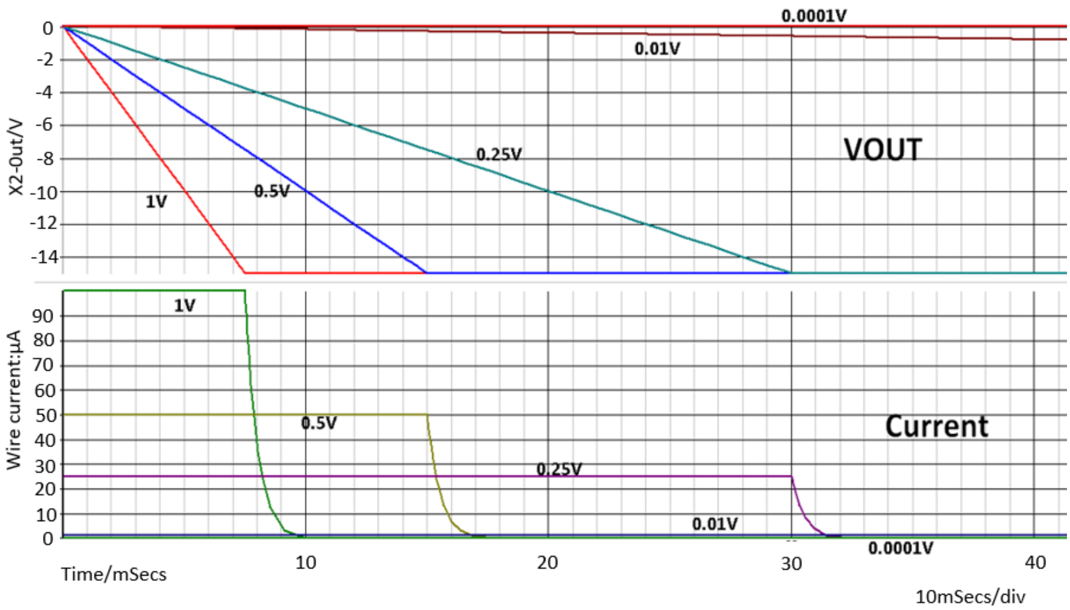

Figure 3- 35: Vout vs charging current

Interestingly, the smaller the charging current, the slower the rate of change of the output.

Note that the inverting input is held at zero volts. This make sense if the rate of change is very small for an input voltage which is near at zero volts. However, there can be a very small input leakage current that can still charge the capacitor and generates very slow slew rate.

3.6 Resonant filter limitation on PFM switching regulators

Resonant filter is effective on filtering the fundamental ripple of switching regulator as long it's operating in PWM. This is due that the fundamental ripple frequency is the same as with the switching frequency of the switching regulator. In addition, the switching frequency does not change with respect to the load current. PWM is efficient for medium to high current loads. Any change of load current does not affect the fundamental ripple amplitude. The same goes even for very light loads as long the regulator is forced in PWM operation. This can be done using synchronous FET's. However, in cases such as light loads, PWM operation is sometimes not ideal due to much lower efficiency it can offer. To improve efficiency, using a synchronous buck regulator topology as an example, operation such as PFM or pulse frequency modulation are used. Output waveform operating in PFM is characterized by two different frequency components, the pulse frequency which is defined as the switching frequency of the FET's and the burst frequency which indicates how often the FET switching action goes active after an idle state [36]. In this manner, power loss is reduced since both FET's are off once inductor current reaches to zero (enters discontinuous conduction mode) . However, with this operation, burst frequency is highly dependent to the load current. The output spectral signature is much complicated, wherein burst frequency changes with respect to load current. For very light load, the overall ripple is being dominated by the burst frequency and it resides at very low frequencies where the resonant filter tuning range cannot cover.

3.7 Chapter summary

This chapter presented a novel way of generating resonance through integrating coupled magnetics in a two stage LC low pass filter to significantly attenuate the fundamental output ripple from SMPS. Effects of coupled inductor's DC resistance, its turns ratio and capacitor's ESR towards the filter performance were discussed in detail. An auto-tune resonant circuit using phase lock loop concept was presented to maximize the notch filter effects and always align the given notch frequency to the fundamental output ripple frequency. Barium Strontium Titanate (BST) dielectric capacitor or multi-layer ceramic capacitor are some examples of available tuning element which enable the possibility of resonant tuning. However, the auto-tune resonant filter approach is not effective for SMPS operating in non-steady state or non PWM mode such as PFM where switching frequency is highly variable and dependent on the load.

4

Experimental Platform

4.1 Auto-tune circuit implementation in PCB

4.1.1 Block diagram

In order to successfully aligned the notch frequency to the switching frequency of the buck converter, a tuning circuit is required to counter the effects of component manufacturing tolerance, temperature drift of the coupled inductor and as well as the switching frequency drift of the switching regulator. A phase tuning circuit was implemented in a PCB to evaluate the tuning loop performance between the variable series resonance (formed by the variable capacitor and the mutual inductance of the coupled inductor) and an injected fixed frequency ripple signal from a SMPS. See Figure 4- 1 for the block diagram of the auto tune circuit.

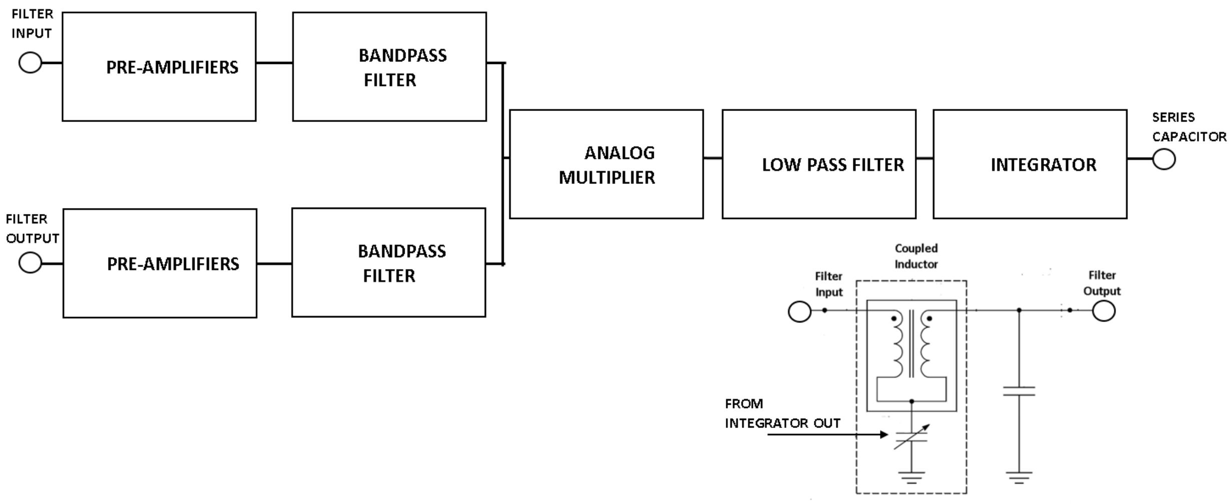

Figure 4- 1: Block diagram of auto-tune circuit

An AC coupled pre-amplifiers were used to amplify the ripple signal for both input and output of the coupled-magnetic filter. Gain can be set through feedback resistors in order to estimate the required amplitude not to further saturate the amplifier input supplies (avoid maximum input rails swing) while still able to provide a discernible signal that can be detected by the phase detector. The critical signal is the signal coming from the output of the coupled-magnetic filter because of its very low amplitude. A bandpass filter (simple first order low pass and high pass filter-RC) is designed to allow a certain pass band frequency range while eliminating other unwanted harmonic frequencies. In this case, the design range targets the switching regulator switching frequency. The analog multiplier serves as the phase detector where it will produce a zero error output when it detects a 90 degree phase shift between the first and second inputs of the analog multiplier to facilitate the alignment of the notch frequency to the fundamental ripple frequency of the switching regulator.

4.1.2 Circuit design

Figure 4- 2 shows the overall auto-tune circuit diagram [21].

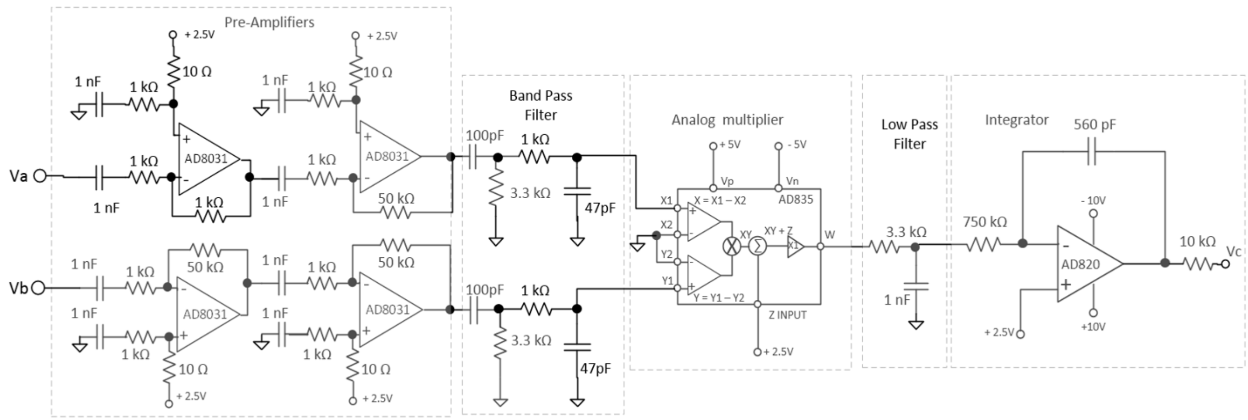

Figure 4- 2: Auto tune schematic circuit

While Figure 4- 3 shows the coupled inductor filter circuit diagram in two possible ways.

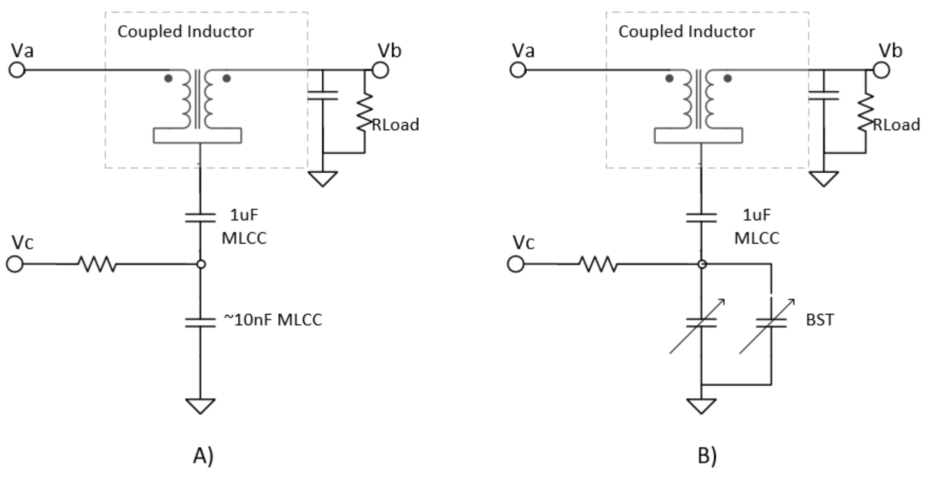

Figure 4- 3: Coupled inductor with variable capacitance A) MLCC B) BST

The coupled inductor filter input, Va is the input terminal to the output of the switching regulator. While Vb is the input terminal of the coupled-magnetic filter output. Vc is the input terminal where the integrator output will drive the variable capacitor to correct and align the resonance in accordance to the fundamental frequency of the output ripple.

Coupled inductor filter input and output signal is AC coupled and amplified through two amplifier stages as depicted in Figure 4- 4 using AD8031 rail to rail I/O amplifier [37].

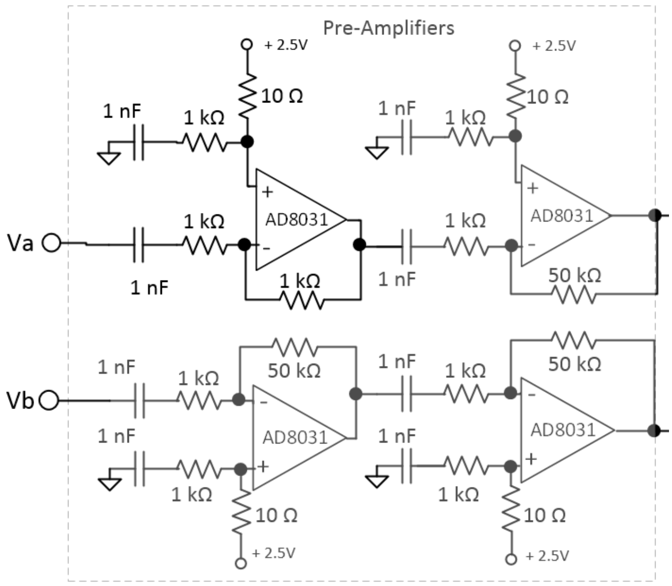

Figure 4- 4: Pre-stage amplifiers

These are low noise amplifiers where its operation is to amplify the input and output signals of the coupled inductor filter. Only one amplifier is used for the coupled inductor filter input due to its relatively large ripple signal compared to its filtered output. Note that gain and input voltage supply should be considered for the signal not to exceed the input supply voltage value. In this case a gain of 50 is used for the input signal of the coupled inductor filter. However, on the signal at the output of the filter is quite more challenging to detect. Moving to resonance point will further attenuate the signal. Two inverting cascaded amplifiers with a gain of 50 each were used.

The amplified signal was filtered using a single pole bandpass filter as shown in Figure 4- 5. These filters are combination of a high pass and low pass RC filter with cut-off frequencies of 482 kHz and 3.3 MHz passing the range of frequency within the specified cut-off. The fundamental ripple frequency is within the pass band.

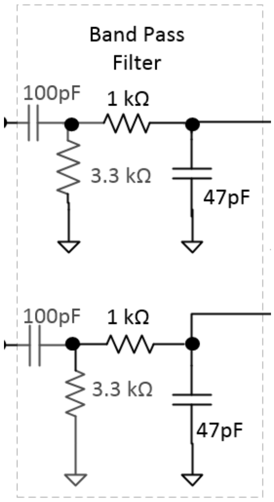

Figure 4- 5: Bandpass filter

The amplified and filtered input and output signals are then fed to analog multiplier, ADN835 as shown in Figure 4- 6 [38]. AD835 uses 4 quadrant voltage output which serves as the phase detector. The part will produce a zero error output when it detects a 90 degree phase shift between the first and second inputs of the analog multiplier. This facilitate the alignment of the resonant notch to the fundamental ripple frequency of the switching power supply. The output basic function is depicted in (18).

$$W = XY + Z \tag{18}$$

Where *W* is the output of the multiplier, *X* and *Y* are the inputs and *Z* is the offset voltage.

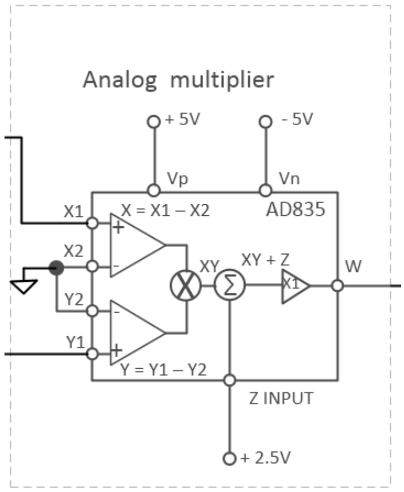

Figure 4- 6: Analog multiplier

After the multiplier, if furthers removes high frequency noise through the RC low pass filter. The output of the RC filter is an error which is fed to the input of the integrator circuit shown in Figure 4- 7. The integrator is AD820 is a single supply rail-to-rail operational amplifier [39]. The circuit integrates the error from the multiplier output. It drives the variable capacitor to vary the resonance in alignment with the fundamental ripple frequency. The error approaches to zero if the resonant frequency locks on the fundamental ripple frequency. The inverting terminal value should be equal or very close to the input supply of the non-inverting terminal.

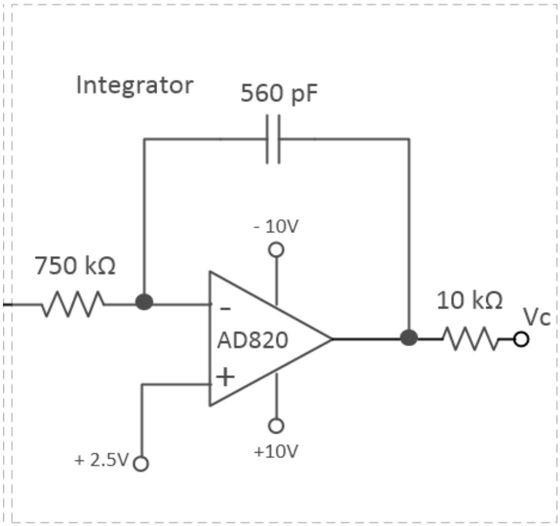

Figure 4- 7: Integrator

4.1.3 Board prototype schematic and lay-out

Actual photo of the auto-tuning PCB is shown in Figure 4- 8.

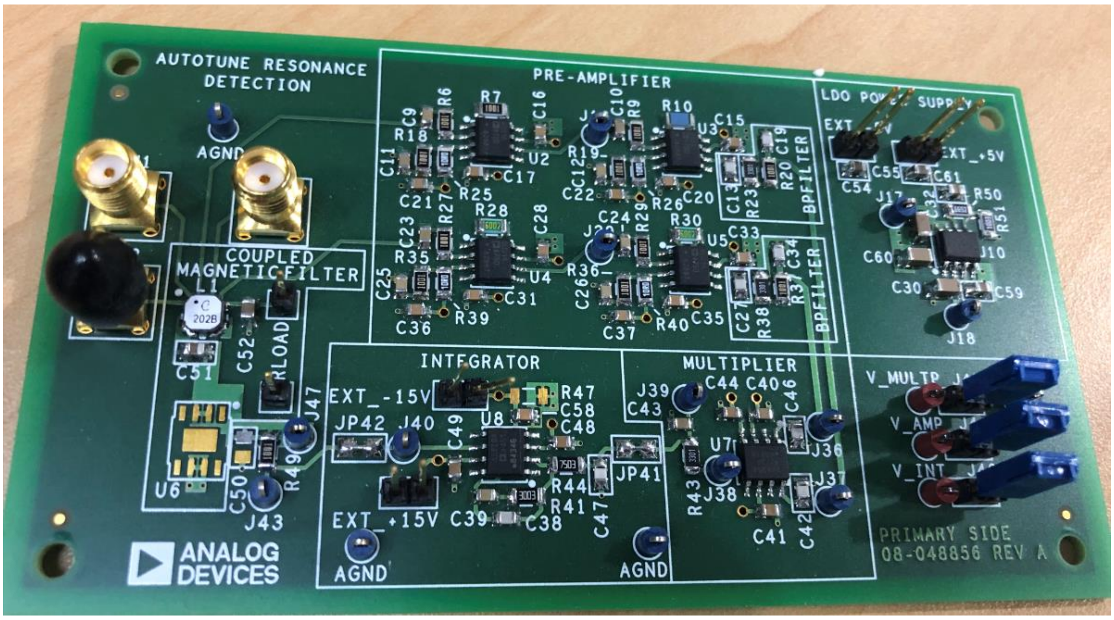

Figure 4- 8: Auto tune prototype board

Auto tune Resonance Detection board Schematic

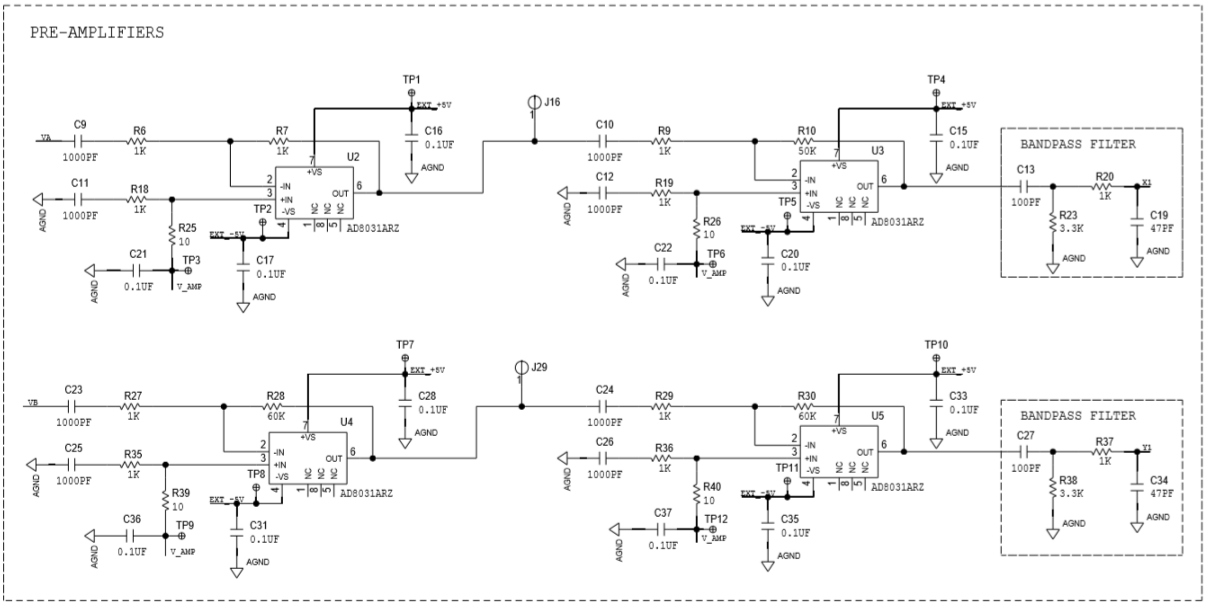

Figure 4- 9: Pre-stage amplifiers

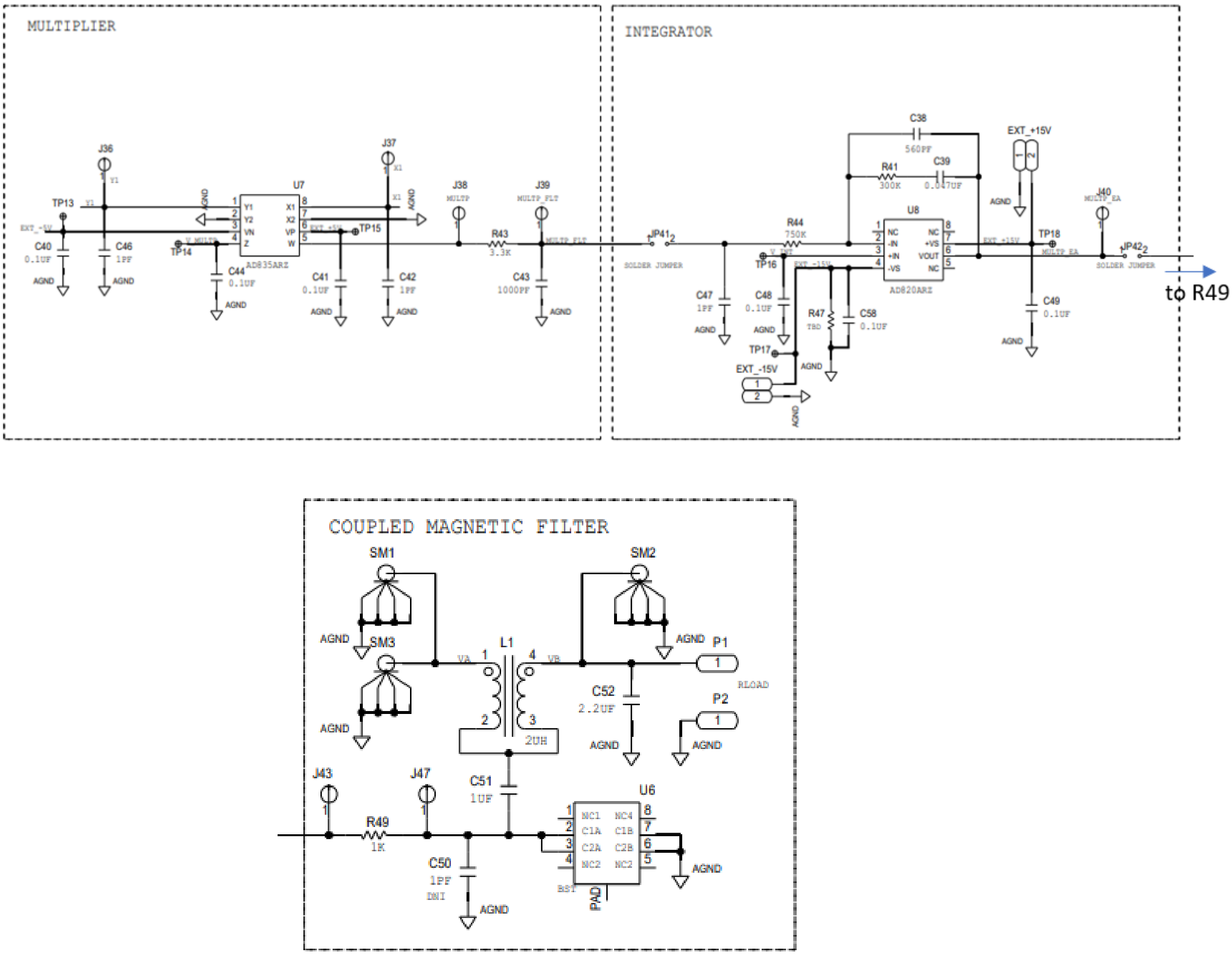

Figure 4- 10: Multiplier, integrator and coupled-magnetic circuit

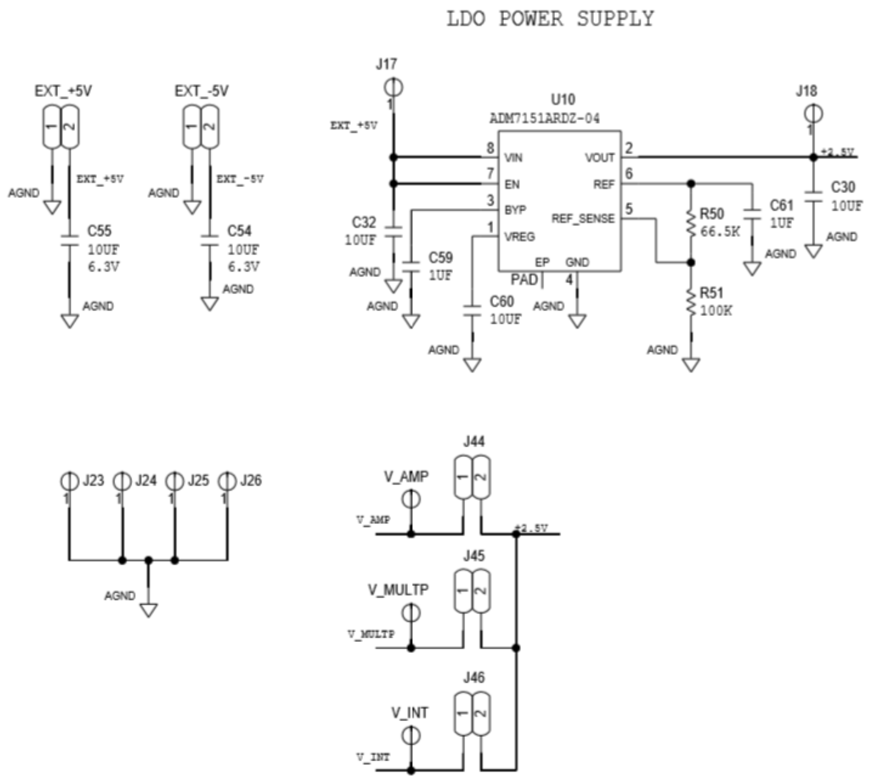

Figure 4- 11: LDO for driving 2.5V DC biasing to multiplier, integrator and pre-stage amplifiers

The 4 layer board layout are depicted below.

Top layer

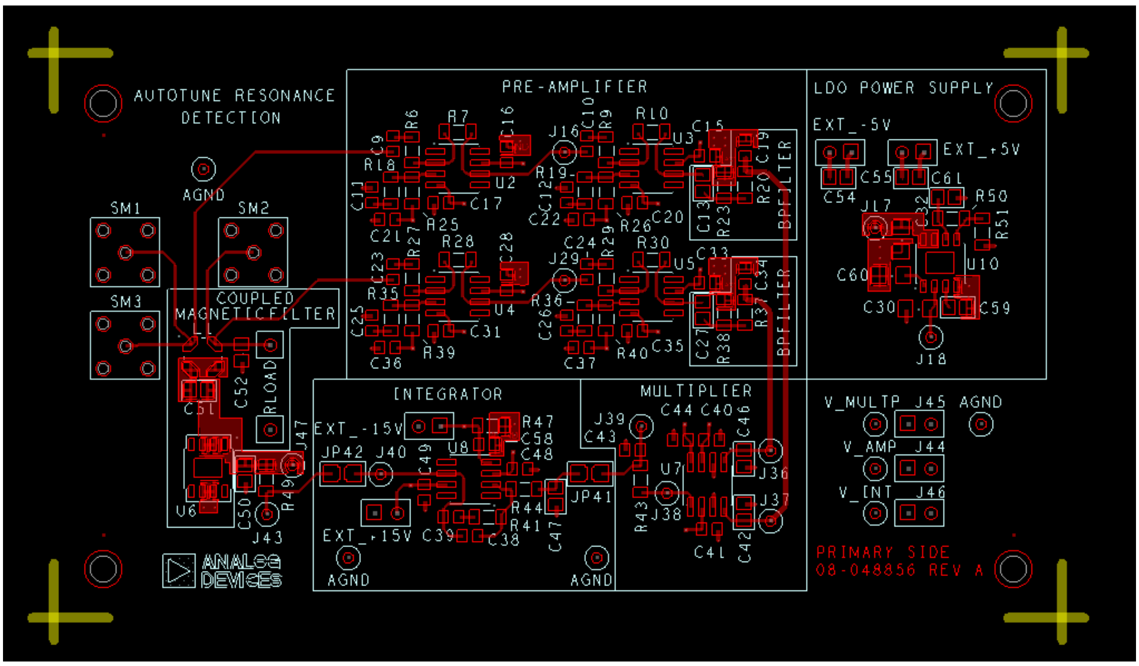

Figure 4- 12: Top Layer

Ground layer

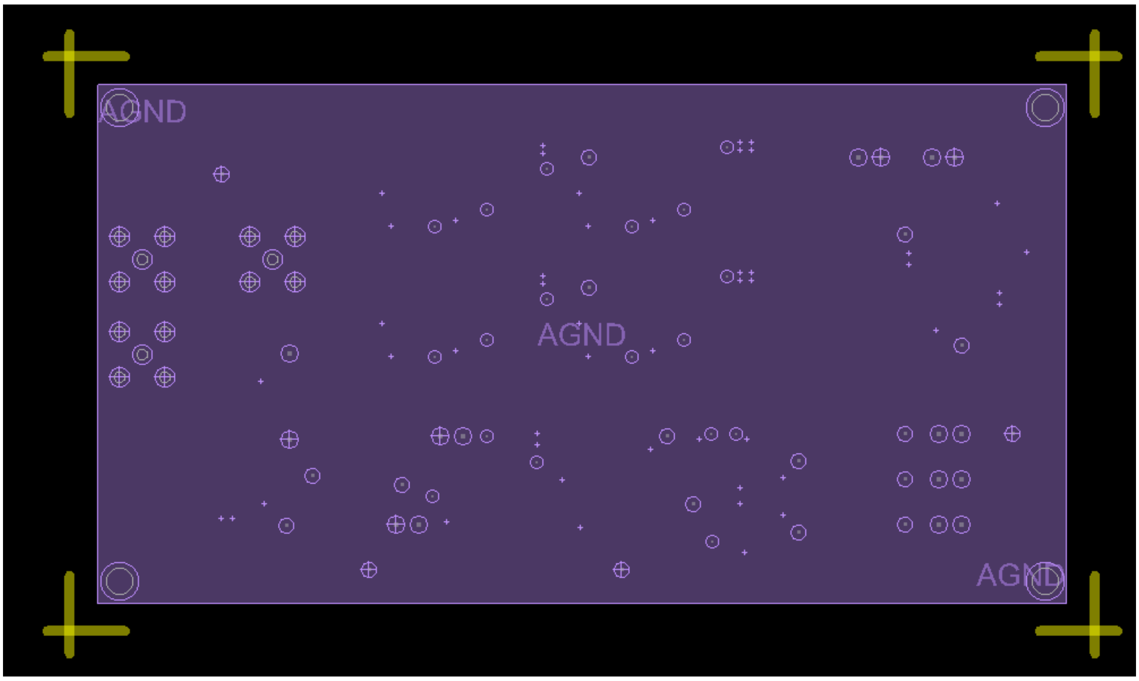

Figure 4- 13: Ground or second layer

3rd Inner layer

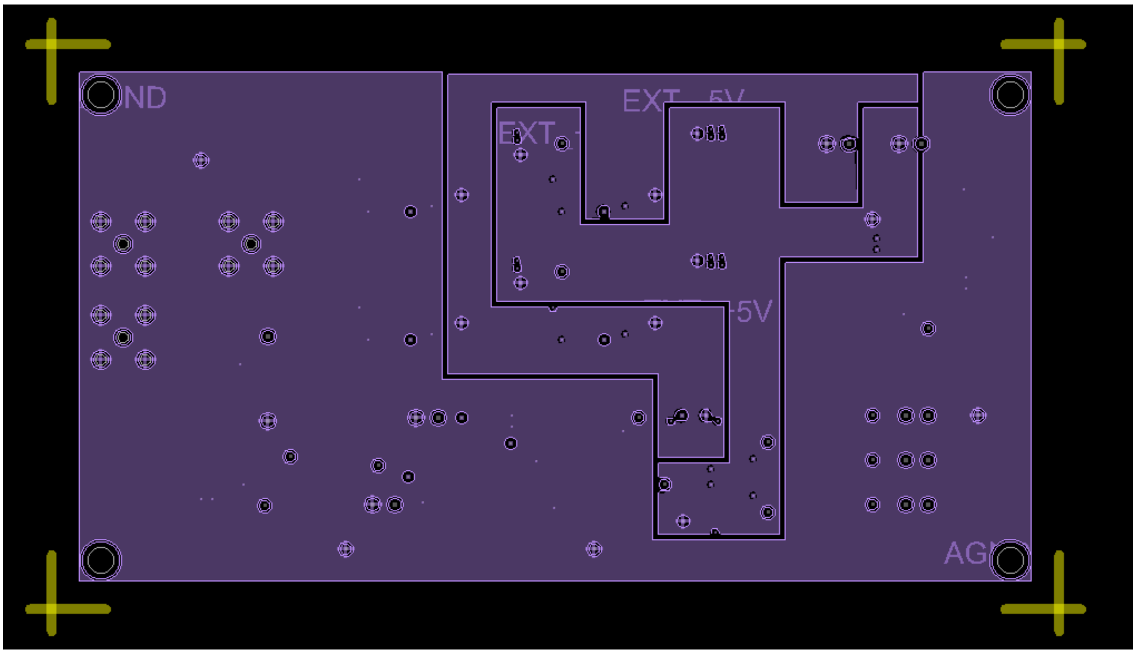

Figure 4- 14: 3rd layer comprising additional power path

Bottom Layer

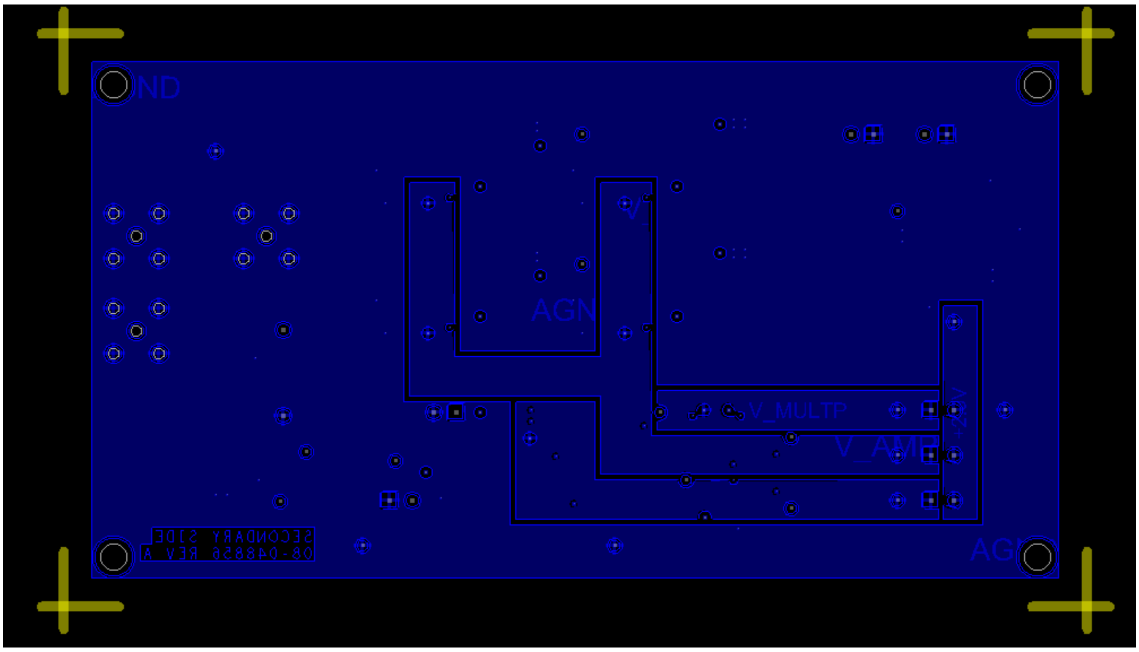

Figure 4- 15: Bottom layer

4.2 BST fabrication

A BST IC die is fabricated using two 0.2 um BST dielectric thickness capacitors housed in an 8 lead SOIC package with paddle size of 95 x 130mm. The same BST material is used in Varactor-Based Passive Ripple Filter With Automatic Tuning for Low-Noise Power-Supply Systems, IEEE Transactions on Power Electronics [21].

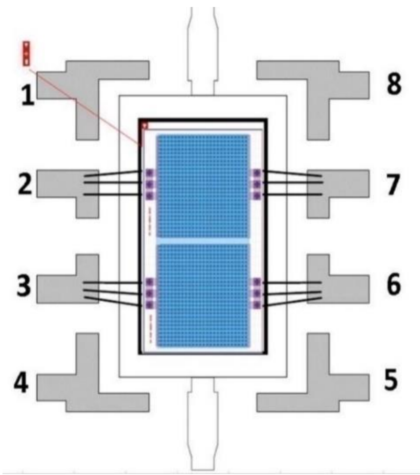

Figure 4- 16: BST sample prototype bonding diagram

Electrical performance specification in terms of breakdown voltage, tuneability, Q factor, relative permittivity, capacitance density and maximum capacitance change are depicted below:

- Breakdown Voltage = 18V
- Tunability defined as the ratio of maximum capacitance over the minimum capacitance is 3.05 from 0 to 10V control voltage range
- Quality factor defined as the ration of capacitive reactance over the equivalent resistive loss (ESR) is 20 at 1 GHZ.
- Relative permittivity is 475
- Capacitance density is 20fF/µm^2
- Capacitance change at temperature change from 0C to 25C is 22%

Key BST specification for resonant tuning application is the tuneability range which dictates the allowable frequency range it can cover. The Q factor on the other hand is also important. Higher Q is preferred to provide a much deeper notch rejection at the resonant frequency.

Figure 4- 17 shows a die photograph of the BST dielectric comprising two capacitors while the zoom view of the capacitor array elements is shown in Figure 4- 18.

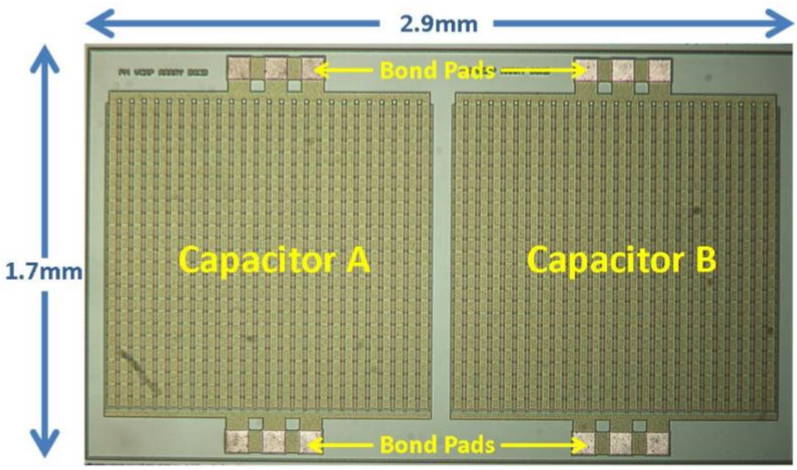

Figure 4- 17: BST array capacitors

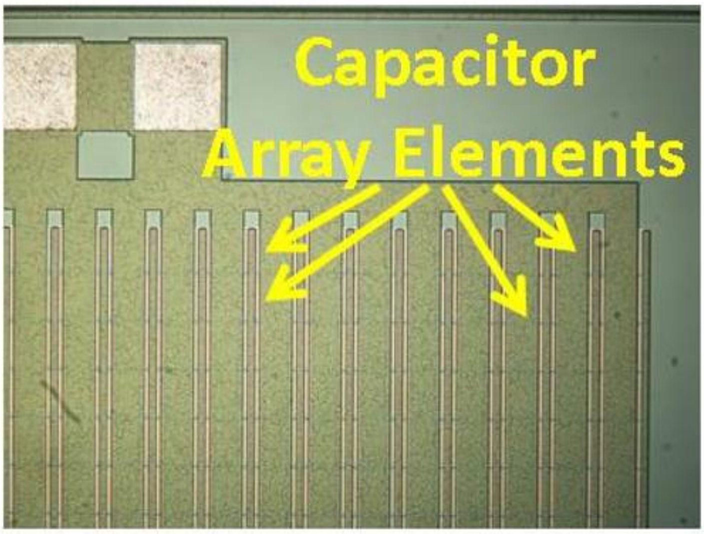

Figure 4- 18: Capacitor array element

Figure 4- 19 shows the cross-sectional view of the 0.2µm BST using a scanning electron microscope.

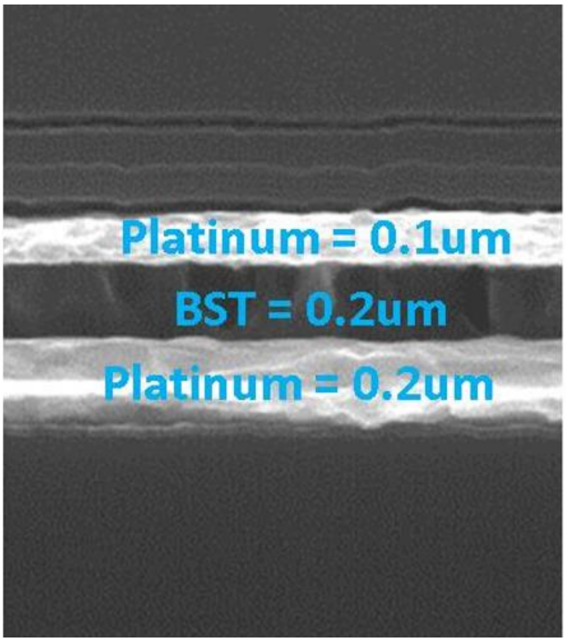

Figure 4- 19: Cross sectional area of sample BST prototype

5

Test Methodology and Experimental Results

5.1 Notch filter response using coupled inductor integrated in two stage LC low pass filter

An insertion loss or forward transmission characteristic test was performed using a network analyser to prove that there is really a notch filter formation when an off the shelf coupled inductor filter and an off the shelf ceramic capacitor were configured as shown in Figure 5- 1.

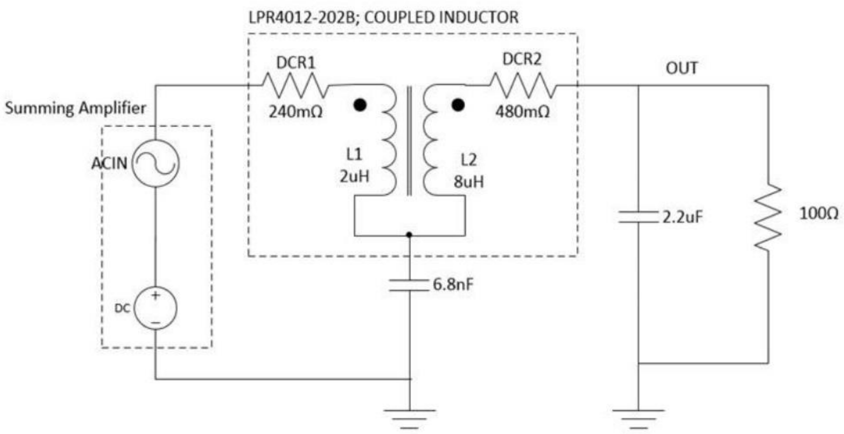

Figure 5- 1: Bench test set-up

The coupled inductor (Coil Craft) has turns ratio 1: 2 with primary inductance of 2uH (tolerance of +/- 20%) and coupling coefficient of 0.95 [40]. The secondary inductance is 8uH due to the squared number of turns. The 6.8nF capacitor is a multi-layer ceramic capacitor (MLCC). It has very low ESR (less 10 mΩ) which is very suitable for this filter application. Resistive element should be very low in the shunt path to not dampen the notch response. Therefore, the use of low ESR capacitor is required to increase the filter's quality factor. A summing amplifier (with low output impedance) is used to sum up the AC and DC bias signals. An AC sweep from 100 Hz to 30 MHz was performed to evaluate the filter's response. Figure 5- 2 show the results.

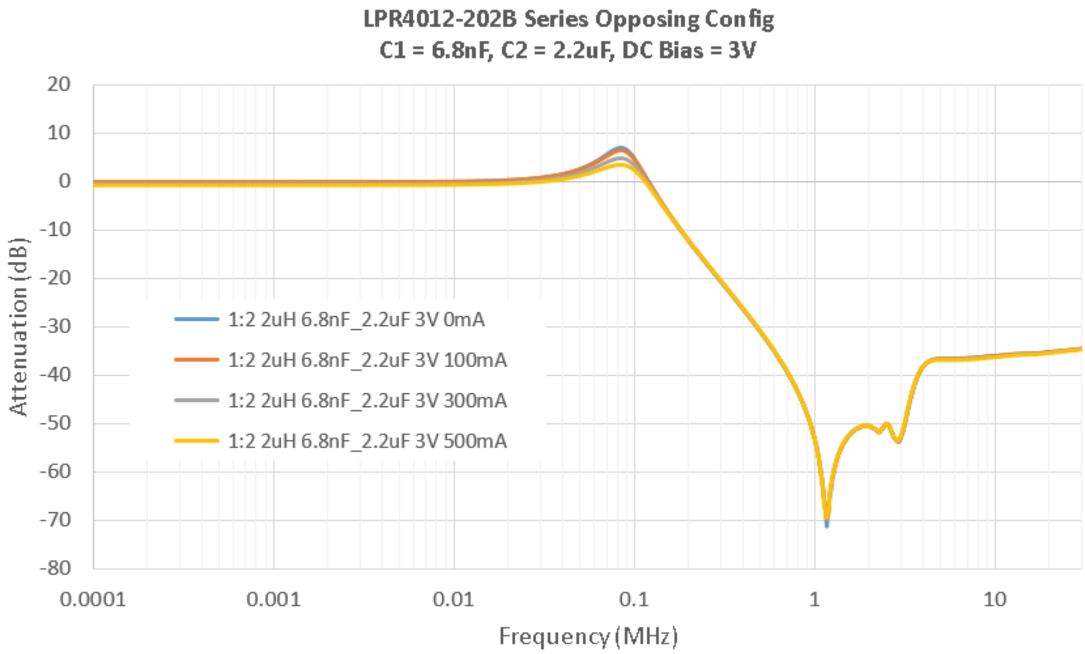

Figure 5- 2: Measured filter response

It can be seen from the results that there is an actual notch response at around 1.15 MHz. The mutual inductance can be calculated using equation (10) where k is the coupling coefficient of 0.95, L1 is the primary inductance of 2uH, L2 is the secondary inductance of 8uH.

The calculated mutual inductance is 3.8µH and the specified capacitance is 6.8nF. The calculated resonant frequency is 990 kHz, not that far from the measured notch frequency at 1.15 MHz if component tolerances are to be accounted for.

The results also show that there were no significant difference of the depth of attenuation at the notch frequency from no load to 500mA load. The depth of the notch frequency is independent with the load and is dominantly dictated by the quality factor of the shunt path.

5.2 Actual test validation on switching regulator

The ADP2114 a dual output step-down switching regulator can be externally synchronized from an external clock ranging from 200 kHz to 2 MHz. First, the resonance created by the mutual inductance and series capacitance was validated in actual application. An off the shelf coupled inductor (Coil Craft) was used with primary and secondary inductance of 2uH and 8uH respectively. Two off the shelf MLCC capacitors

(Murata) were used as the mid-capacitor with capacitance value of 6.8nF and 10nF to test the notch frequency if it resides to two different frequency location. The test configuration can be seen in Figure 5- 3.

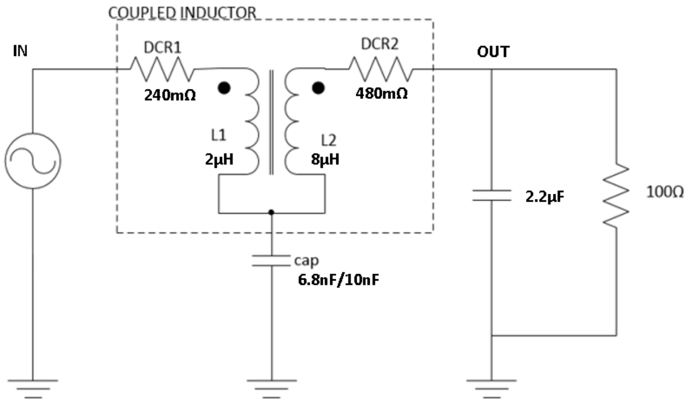

Figure 5- 3: Test configuration insertion loss

Using a network analyser to test the coupled-magnetic filter in figure 5- 3 (1 kHz to 10 MHz) for two different series capacitance value (6.8nF and 10nF) yield the following insertion loss results (Figure 5- 4).

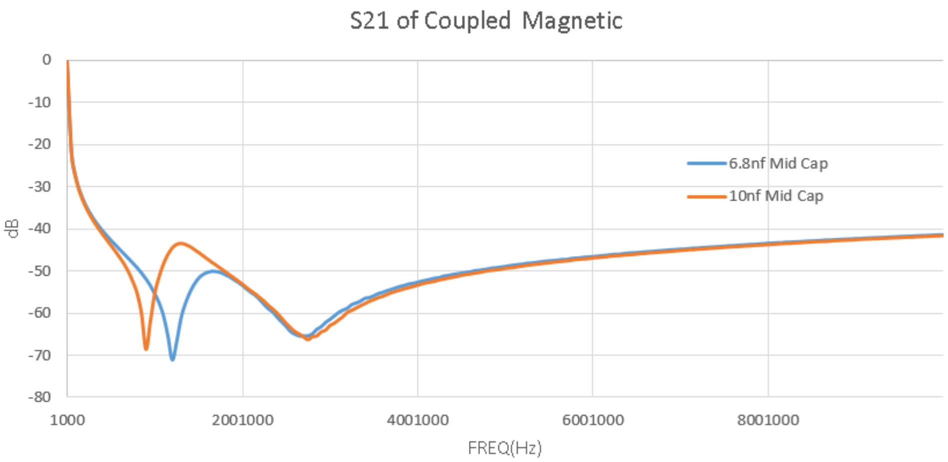

Figure 5- 4: Insertion loss results

The notch frequency changes due to the change of the series capacitance value. Increasing the capacitance moves the notch at lower frequency as expected. The notch frequency can be estimated by calculating the resonant frequency of the mutual inductance formed by the primary and secondary inductance (k = 0.95) and the series capacitance.

The coupled-magnetic filter was applied to the output of a switching regulator in which the switching frequency is aligned to the notch frequency of the filter. The switching regulator is ADP2114, a synchronous step down DC-DC regulator [41].

Results#1 evaluated in Spectrum domain. Using coupled-magnetic filter with 6.8nF series ceramic capacitor after a buck regulator clocked around 1.2 MHz. See Figure 5- 5.

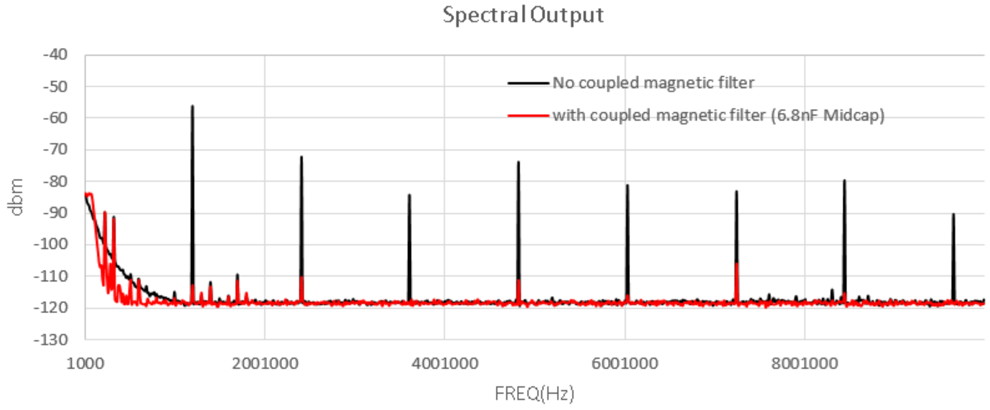

Figure 5- 5: Buck spectral output with and without coupled-magnetic filter running at 1.2 MHz

Results#2 evaluated in Spectrum domain. Using coupled-magnetic filter with 10nF series ceramic capacitor after the buck regulator clocked around 900 kHz. See Figure 5- 6.

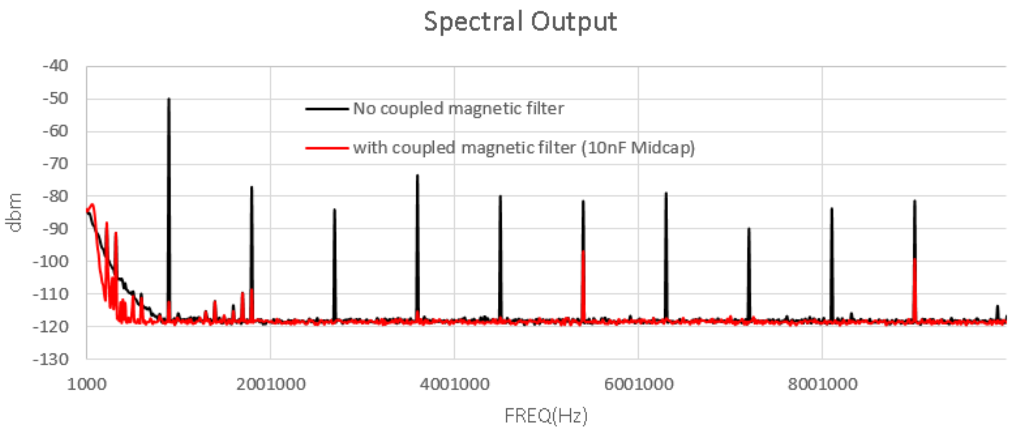

Figure 5- 6: Buck spectral output with and without coupled-magnetic filter running at 900 kHz

There is a significant reduction of the fundamental ripple amplitude of the buck regulator when coupled-magnetic filter is used based from the evaluation results.

5.3 Auto-tune experimental results

5.3.1 Analog multiplier test validation

The analog multiplier section serves as the phase detector where it will produce a zero error output when it detects a 90° phase shift between the first and second inputs of the analog multiplier to facilitate the alignment of the resonant notch to the fundamental ripple frequency of the switching power supply.

Two synchronized signals were injected at the analog multiplier inputs (X1 and Y1). The phase difference was varied across each specified signal amplitude. Figure 5- 7 shows the DC output of the multiplier with respect to varying phase difference between analog multiplier inputs at various specified signal amplitudes.

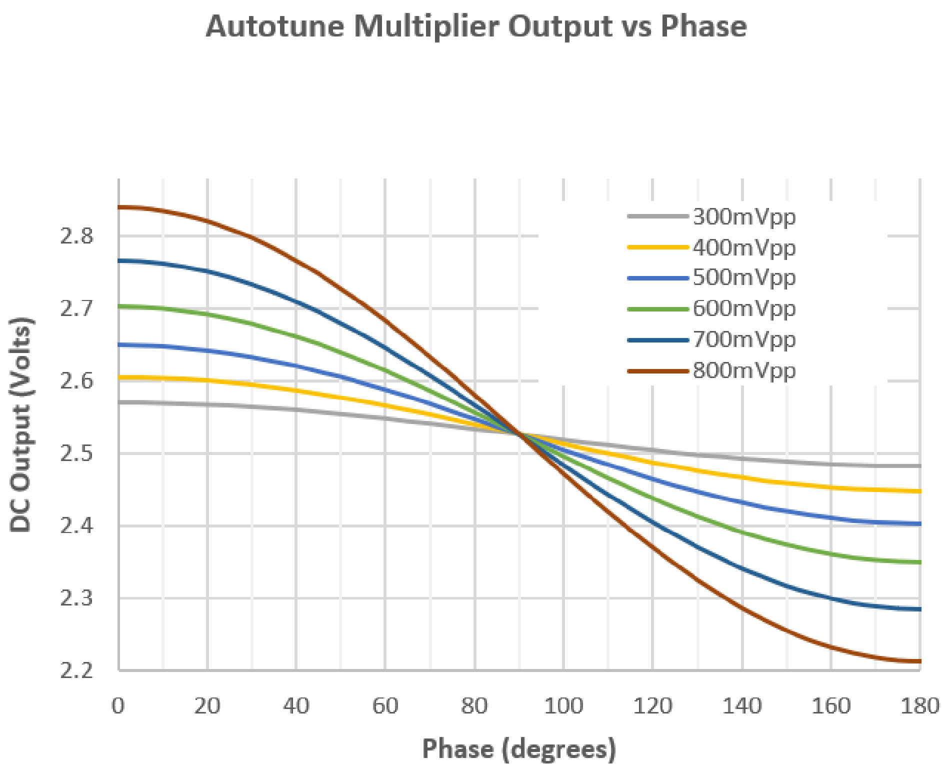

Figure 5- 7: Multiplier output and phase

Characteristics of the curve can also be obtained through the equation:

$$Va * Vb = \frac{A1xA2}{2}[\cos((\emptyset_1 - \emptyset_2\,)] \qquad (19)$$

Where $(\emptyset_1 - \emptyset_2\,)$ represents the phase difference of X1 and Y1multiplier inputs [21].

It was observed that at 90°, the curves meet at a point where the multiplier outputs 2.526Vdc (note that Z input set equals to 2.5Vdc). The difference of 26mV can be accounted as an offset inherent in AD835 part. This also correlates to the equation wherein cosine of 90° would equate to zero. This is the point where maximum attenuation is achieved at 90° phase shift.

5.3.2 Coupled-magnetic filter open loop test validation

An MLCC was used as a variable capacitor to test the open loop of the auto-tune circuit. The capacitor DC bias characteristic at 25°C is shown below (Figure 5- 8). Capacitor used was GRM022R61A103ME19 valued at 10nF [42].

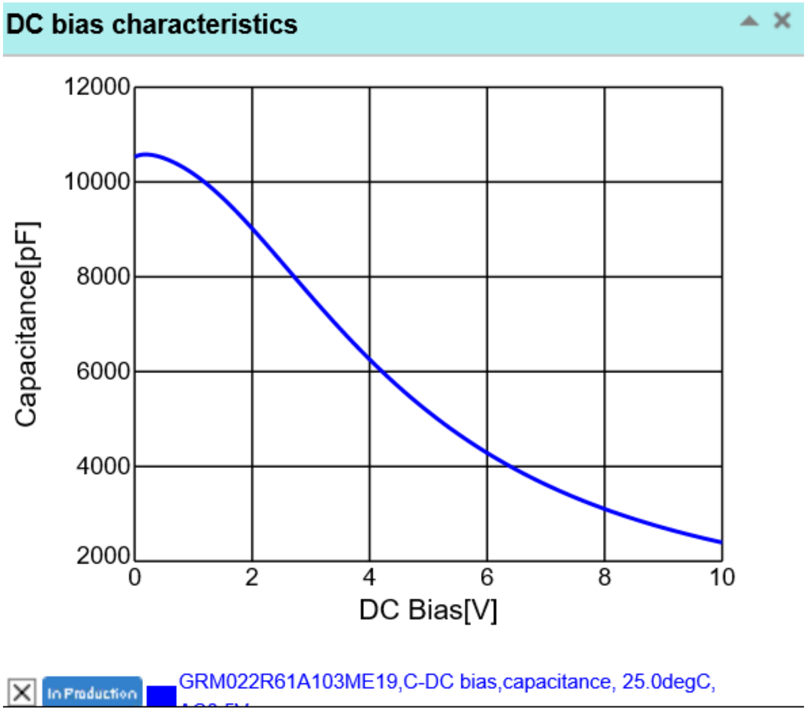

Figure 5- 8: MLCC DC bias characteristics (Murata SimSurfing Tool)

Figure 5- 9 shows the diagram of the open loop test. A sinusoid signal of 1.15 MHz 100mVpp is injected through the coupled-magnetic filter. The control voltage or Vc is varied to evaluate the frequency with greatest attenuation and see if it matches with the injected frequency.

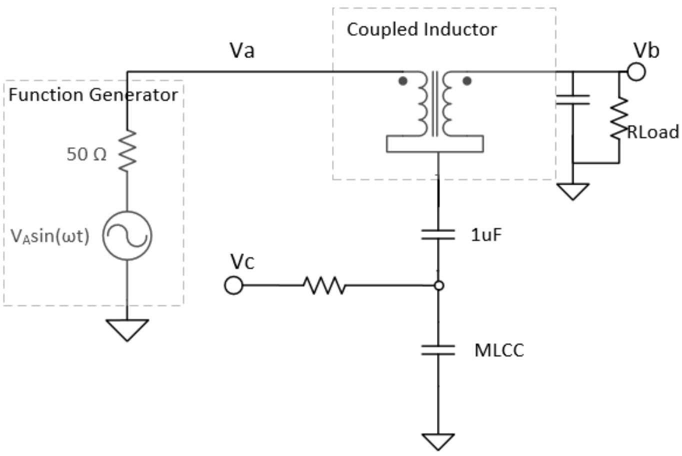

Figure 5- 9: Coupled-magnetic filter with injected sinusoidal wave

Figure 5- 10 shows the results where DC voltage at the filtered multiplier output is measured while simultaneously capturing the amplitude of the injected signal at the output of coupled-magnetic filter through spectrum analyser. This measurement is across sweeping bias voltage across the MLCC. The error is calculated from the Z input voltage where the multiplier inherent offset is factored in.

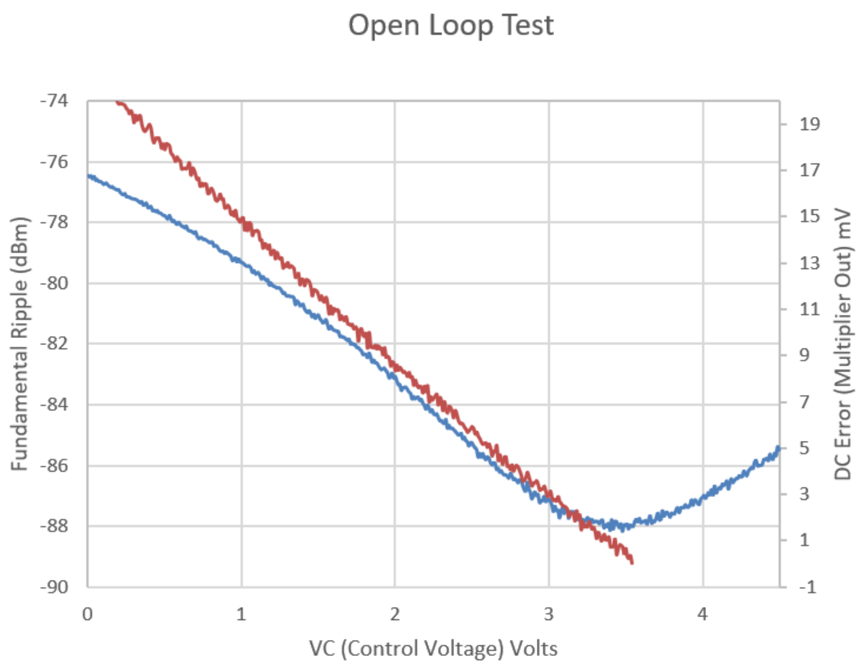

Figure 5- 10: Open loop test results

Results shows that at 3.5V Vc generates the smallest fundamental ripple that can be at the output of the coupled-magnetic filter (Vb). Hence this is also the region where the error is the smallest, approximately 0mV.

5.4 Filter performance comparison of coupled inductor in a two stage LC low pass filter vs. conventional two stage LC low pass filter

5.4.1 Simulation results

Figure 5- 11 shows the schematic circuit and Figure 5- 12 shows the gain vs frequency plot comparison having uncoupled ($k = 0$) and coupled inductance ($k = 0.93$) using the same value of passive components.

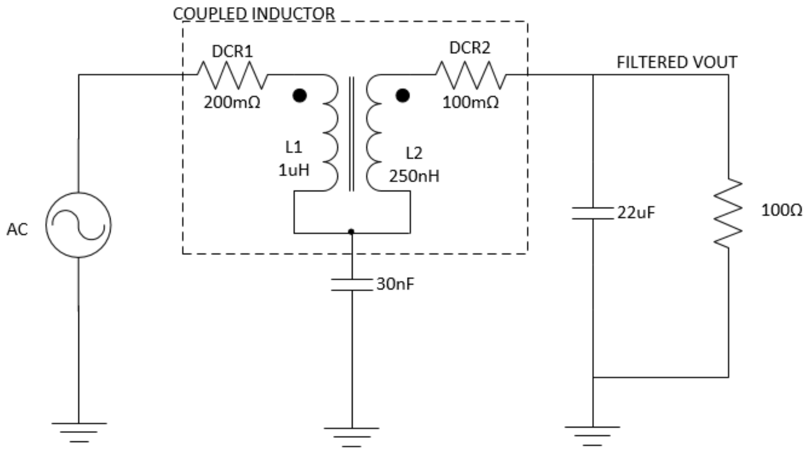

Figure 5- 11: Circuit simulator test circuit for comparison of coupled and uncoupled inductor

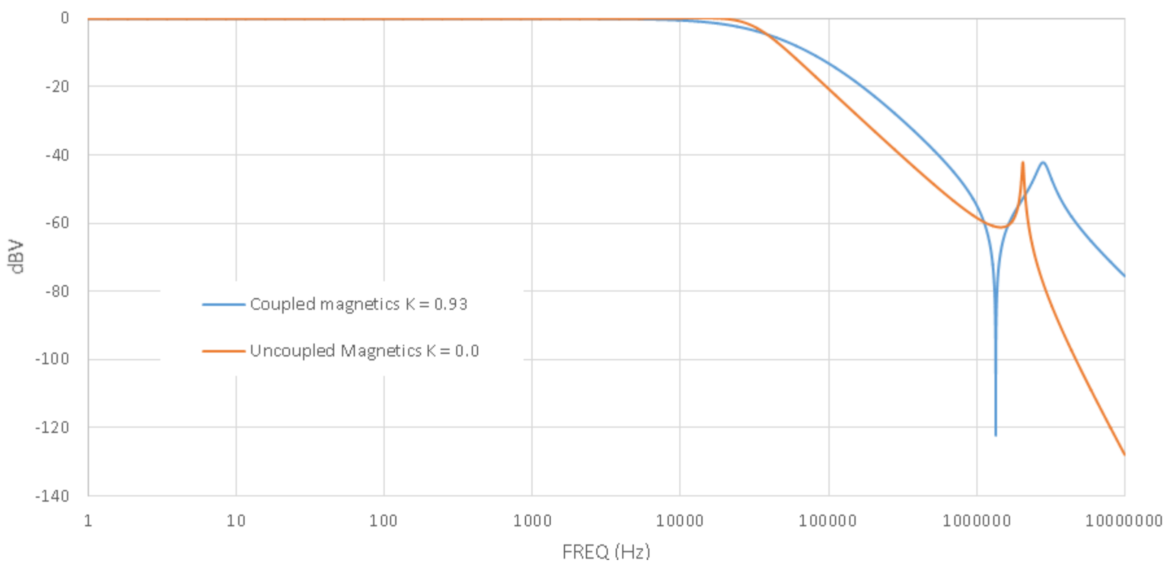

Figure 5- 12: Two stage LC low pass filter transfer function using coupled and uncoupled inductor

In comparison from the conventional LC low pass filter, an off the shelf coupled inductor can be acquired in a single package. Coupled magnetics in a two stage LC filter can provide more reduction on the fundamental ripple frequency as long it coincides with the resonant frequency in comparison with conventional two stage LC filter with less volume and component count

5.5 Challenge encountered on close loop resonant tuning with SMPS

An actual problem encountered by the author is the auto close loop tuning using an actual switching regulator's output ripple. It seems it needs more time and study to investigate why it’s not tuning correctly. Hence, the voltage output of the integrator keeps railing on its maximum power supply voltage. The fundamental output ripple after the filter may be too small to be detected near the resonance. Thus, the author used an “emulated ripple” using an arbitrary waveform generator for testing the actual close loop response. Figure 5- 13 shows a sample close loop results where it locks around 3.4V with very long and impractical delay (more than 10 seconds to reach 3.4V).

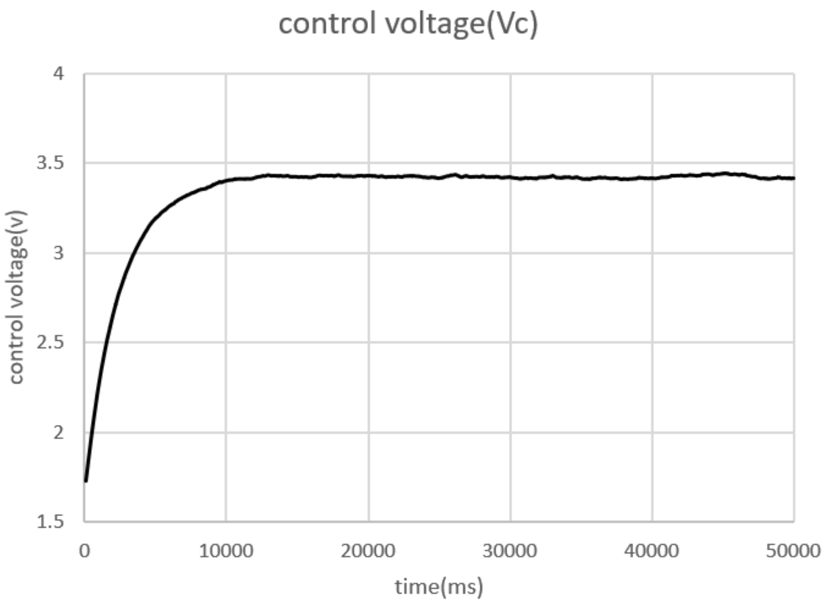

Figure 5- 13: Auto-tuning close loop result

5.6 Chapter Summary

This chapter presented the measurement results of the actual resonant filter using an off the shelf inductor and capacitor and the functionality of the resonant auto-tune circuit. It was validated that there is a generation of a notch filter effect where in the mutual inductance of the coupled inductor and the series capacitance creates the series resonance. This resonant filter was applied to a buck regulator and it proves to be effective at filtering the fundamental output ripple. The auto-tune circuit was evaluated in close-loop and open-loop configuration using an emulated ripple. Open loop test shows good functionality of the circuit while at close loop, it locks at the resonant point with very long and impractical delay.

6

Conclusion and Future Works

In this research work, an obvious detrimental output artefact from SMPS, a buck regulator to be specific is the fundamental output ripple. Effects are seen through various data converters and transceivers, which all boils to performance degradation specifically its AC specifications, i.e. SFDR and SNR for data converters or phase noise for transceivers. Therefore, the fundamental output ripple artefact should be significantly reduced up to a point where it no longer pose a substantial risk to noise sensitive loads or applications.

The fundamental output ripple is predictable when operating at a steady state PWM mode. The frequency is coherently related to the switching frequency where the noise energy is at greatest. Coupled inductor or coupled-magnetic techniques can be applied to a conventional two stage LC low pass filter to form a notch filter response where the notch frequency can be aligned with the fundamental output ripple frequency. The notch filter effect is created due to the series resonance formed by the combination of the mutual inductance of the two coupled inductors and the series capacitance that were validated on both simulation and actual test. A simulation comparison was done over a typical conventional two stage LC low pass filter wherein both inductors are uncoupled (coupling coefficient is zero). The coupled inductor technique resulted a significant advantage over a conventional two stage LC low pass filter in terms of fundamental ripple attenuation at discrete frequency.

To validate the effectivity of the technique, the coupled-magnetic concept in two stage LC low pass filter was applied after an actual buck regulator. The switching frequency was synchronized to the calculated series resonance. The fundamental output ripple is significantly attenuated after the filter at around 60dB. A low ESR ceramic capacitor was used since the level of attenuation highly depends on the Q or quality factor of the series resonance.

An auto-tune circuit using phase-lock loop concept was designed and developed to test the tracking ability of the variable resonant filter to the fundamental ripple frequency of SMPS. Two variable capacitor components were discussed that can help generate variable resonant frequencies. Barium Strontium Titanate dielectric capacitor which changes the capacitance over specific DC voltage range or an off the shelf multi-layer ceramic capacitor which has decreasing exponential behaviour of capacitance change over DC bias voltages. An open loop test for the tuning circuit was performed using an off the shelf ceramic capacitor and was proven to be functional.

Future works for this research are as follows:

1. In depth investigation of close loop response testing of in terms of loop stability for the auto-tune circuit with variable capacitor applied on the output of a switching regulator.
    a. Speed of recovery in terms of temperature or switching frequency drift
    b. Transient response of regulation across load steps
2. A limitation of this filter technique is poor point of load regulation specifically at high load currents. The feedback mechanism in this study only relates to the tuning of resonance in accordance to the fundamental ripple frequency. However, the feedback mechanism of the voltage output after the filter is not considered. Hence, voltage drop across the DCR of the coupled inductor are not compensated since these are placed outside the feedback loop of the switching regulator. A further study can be incorporated to implement the coupled inductor technique within the feedback loop of the SMPS.

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Appendices

Appendix A

Output Ripple Measuring Technique published by the Author which paved him to deep dive on the research.

ANALOG DEVICES

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APPLICATION NOTE

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Measuring Output Ripple and Switching Transients in Switching Regulators

by Aldrick S. Limjoco

INTRODUCTION

Minimizing output ripple and switching transients is very important for some applications, especially noise sensitive devices such as high resolution ADCs. When using a switching regulator as a power supply, the output ripple can appear as a distinct spur on the ADC's output spectrum, affecting its dynamic performance, or signal-to-noise ratio and spurious-free dynamic range (SFDR). Due to these undesirable output signals, a switching regulator is sometimes replaced with a low dropout (LDO) regulator. Thus, the high efficiency advantage of the switching regulator is traded for the cleaner output of the LDO regulator. Quantifying these artifacts correctly provides a better perspective when applying, designing, and integrating switching regulators in a wider range of high performance applications and noise sensitive systems.

This application note describes effective techniques for measuring output ripple and switching transients in switching regulators. Measuring these artifacts requires great care because poor measurement setup can lead to incorrect readings. Loops formed by the oscilloscope probe signal and ground leads introduce parasitic inductance. This inaccurately increases the amplitude of switching transients that are associated with the fast switching transitions. Therefore, proper connections and good measurement techniques in a wide bandwidth measurement are observed.

The Analog Devices, Inc., part used to demonstrate the techniques for measuring output ripple and switching noise is the ADP2114 dual 2 A/single 4 A synchronous step down dc-to-dc converter. This buck regulator provides high efficiency and operates at a switching frequency of up to 2 MHz.

Figure 1. Output Ripple and Switching Transients

Appendix B

Published an article towards deep view on the sensitivity and effect of power supply noise to ADC.

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TECHNICAL ARTICLE

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Silent Switcher μModule Regulators Quietly Power GSPS Sampling ADCs in Half the Space

Aldrick Limjoco, Patrick Pasaquian, and Jefferson Eco
Analog Devices, Inc.

High speed analog-to-digital converters (ADCs) have evolved into the gigasamples per second (GSPS) realm, with a corresponding increase in serviceable bandwidth. These performance improvements come with a number of challenges, one of which is more complex power supply requirements. For example, the AD9625, a 2.6 GSPS ADC, requires seven independent power rails, divided into three voltage levels: 1.3 V, 2.5 V, and 3.3 V.

The complete ADC power system must be efficient, fit on an already crowded PCB, and produce output noise that matches the sensitivity of the load. Balancing these requirements, often at odds with each other, is an overriding parametric optimization problem for the system designer. Conventionally, the problem is solved by combining switching regulators—noisy, but efficient—with low dropout (LDO) postregulators, which can be relatively inefficient, but they reduce power supply noise. Figure 1 shows the block diagram for a typical system.

Unfortunately, efficiency and noise-performance optimization usually come at the expense of system complexity. Figure 2 shows an alternative power system using μModule® Silent Switcher® regulators. This solution provides quiet power to the ADC in less space and is more efficient than the conventional solution.

Consider Noise

A system designer must consider quantifying the sensitivity of the load and be able to match it to the power supply noise. Power supply noise can be minimized by using a LDO regulator in the power supply path, either as a standalone regulator (Figure 2), or as a postregulator following a switching regulator as shown in Figure 1. An LDO regulator has the ability to reject input supply noise—measured as its power supply rejection ratio (PSRR).

The trade-off to improved noise performance with LDO regulators is lower efficiency. LDO regulators are inefficient at high step-down ratios, as they must dissipate excess power across a pass element, so the goal when using LDO regulators is to minimize the step-down ratio to maximize efficiency. This is why they are often used as post-regulators following inherently noisy, but efficient, switching regulators, which initially step-down a main rail before LDO regulator inputs. Nevertheless, when used as a postregulator, maximizing the PSRR performance of the LDO regulator requires extra headroom, further degrading overall power supply efficiency, especially at higher loads.

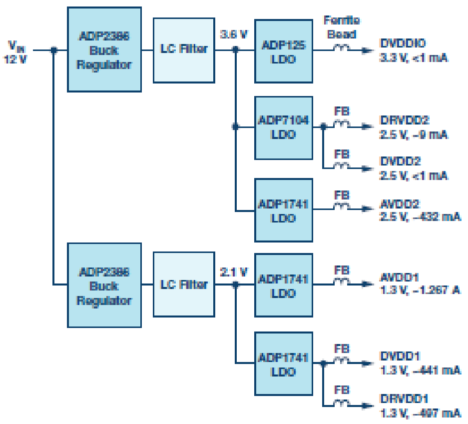

Figure 1. Baseline GSPS ADC power supply design using switching regulators and LDO regulators (conventional design).

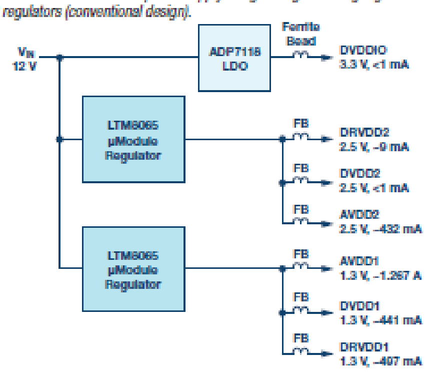

Figure 2. An alternative to the conventional switchers and LDOs power system shown in Figure 1. This design features two LTM8065 μModule Silent Switcher regulators directly powering an AD9625. This design is quiet, more compact, and more efficient (LTM8065 unfiltered design).

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Appendix C

Patent granted on coupled-magnetic technique implemented in a 2 stage LC low Pass filter

US010320280B2

(12) **United States Patent**
Limjoco et al.

(10) **Patent No.: US 10,320,280 B2**
(45) **Date of Patent: Jun. 11, 2019**

(54) **LC FILTER INCLUDING COUPLED INDUCTORS FOR REDUCING RIPPLE IN SWITCHING POWER SUPPLIES**

(71) Applicant: **Analog Devices Global Unlimited Company**, Hamilton (BM)

(72) Inventors: **Aldrick S. Limjoco**, Dasmarinas Cavite (PH); **Jefferson Albo Eco**, Gen. Trias Cavite (PH)

(73) Assignee: **Analog Devices Global Unlimited Company**, Hamilton (BM)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **15/804,437**

(22) Filed: **Nov. 6, 2017**

(65) **Prior Publication Data**

US 2018/0131267 A1 May 10, 2018

Related U.S. Application Data

(60) Provisional application No. 62/419,252, filed on Nov. 8, 2016.

(51) **Int. Cl.**

H02M 1/14	(2006.01)
H02M 3/155	(2006.01)
H03H 7/01	(2006.01)
H02M 1/15	(2006.01)
H02M 1/00	(2006.01)

(52) **U.S. Cl.**
CPC ***H02M 1/143*** (2013.01); ***H02M 3/155*** (2013.01); ***H03H 7/0115*** (2013.01); *H02M 1/15* (2013.01); *H02M 2001/0064* (2013.01); *H03H 2210/025* (2013.01)

(58) **Field of Classification Search**
CPC H02M 1/143; H02M 3/155; H02M 1/15; H02M 2001/0064; H02M 7/523; H03H 2210/025; H03H 7/0115
See application file for complete search history.

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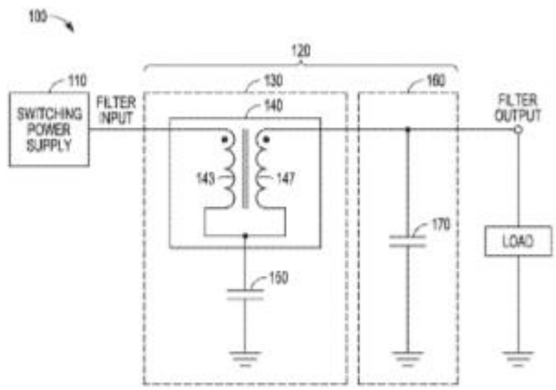
Primary Examiner — Fred E Finch, III
Assistant Examiner — Demetries A Gibson
(74) *Attorney, Agent, or Firm* — Schwegman Lundberg & Woessner, P.A.

(57) **ABSTRACT**

An LC filter circuit reduces an output voltage ripple of a switching power supply using coupled inductors in combination with a capacitor to form a notch filter, and aligning the notch region of the notch filter with a ripple frequency of the switching power supply to attenuate the frequency region of the fundamental ripple frequency by a larger amount than other frequencies.

20 Claims, 8 Drawing Sheets



Appendix D

BST Verilog-a Text

```
// VerilogA for BST_model, BST, veriloga


`include "discipline.h"
`include "constants.h"

module BST(p, n, vc);

inout p, n;
input vc;
electrical p, n, vc;

parameter real p0=8.5;
parameter real p1=0.03922;
parameter real p2=-0.32832;
parameter real p3=-0.00069;
parameter real p4=0.00906;
parameter real p5=-0.00001;
parameter real p6=-0.00009;
parameter real r=0.003;
parameter real l=900p;
real Vd, c;

analog begin
Vd = V(vc);

c = (p0 + p1*pow(Vd,1) + p2*pow(Vd,2) + p3*pow(Vd,3) + p4*pow(Vd,4) +  p5*pow(Vd,5) + p6*pow(Vd,6))*0.000000001;
V(p,n) <+ r*I(p,n) + l*ddt(I(p,n)) + idt(I(p,n))/c ;

end

endmodule
```

USE File

*testsim.use

```
keep all

sim test.ckt

sweep freq from 10 to 100e7 dec 100

go
```

Appendix E

Schematic test netlist

*testsim.use *test.ckt

```
*
****************************************************
* Adice5 Netlist for Block TEST_BENCH,TEST,schematic
* CAD_PROCESS        :: "l50_bcd_db_1p5mu_1p8v_5v_40v"
* CAD_PROCESS_MAINVER:: "31.10"
* CAD_PROCESS_TOOLVER:: "cadenceoa/31.10"
* CAD_PROCESS_VER    :: "31.10"
* CAD_FOUNDRY        :: "-"
* CAD_FOUNDRY_VER    :: "-"
* CAD_OPTIONS        :: "MIMCAP=1ff"
* CAD_GENERIC        :: "generic"
* CAD_GENERIC_VER    :: "7.1"
* CAD_PATHS_UPSEARCH :: t
* CAD_PATHS_VERSION  :: nil
* adiceSimViewList   :: ("adice" "schematic" "symbol")
* Netlister Warnings :: ( )
* Netlist-mode       :: "Complete"
* User               :: "alimjoco@alimjoco-lx01.adgtdesign.analog.com"
* Netlister version  :: "1.28 (Date: 2017-05-03 10:41:54-04)"
* Date               :: "May 16 11:48:29 2017"
* CadenceSession Age :: "1hr 20mins 50secs"
* WorkStation upTime :: "3weeks 3days 18hrs 40mins 16secs"
* Pwd                :: "/home/alimjoco/Desktop/MAsters/adice5/TEST"
* "@(#)$CDS: virtuoso version 6.1.7-64b 12/01/2016 05:43 (sjfhw306) $"
****************************************************

****************************************************
* Reference Libraries:
*    ("simulation" "/cad/adi/apps/adi/cic_overlay/current/local_oa/cdsLib/simulation")
*    ("BST_model(l50_bcd_db_1p5mu_1p8v_5v_40v)" "/home/alimjoco/Desktop/MAsters/BST_model")
*    ("TEST_BENCH(l50_bcd_1p5m_1p8v_5v_40v)" "/home/alimjoco/Desktop/MAsters/TEST_BENCH")
****************************************************

****************************************************
*   Top-Block: TEST_BENCH TEST schematic
*  Last Saved: "May 16 11:48:25 2017"
****************************************************
i1:i_sin p:GND n:i1_N dc=0 acmag=1 acphase=0.0 offset=0.0 amplitude=1 &
 freq=1 delay=0.0 theta=0.0 phi=0.0 npts=100 freq2=1
i3:BST n:GND p:i1_N vc:v7_P
r5:r B:GND A:i1_N noise=1 tc1=0 tc2=0 value=100G
v7:v p:v7_P n:GND dc=3.5 acmag=0.0 acphase=0.0

* End Adice5 netlist: ("TEST_BENCH" "TEST" "schematic")
```