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The design and implementation of animal auto identification systems for application within the agricultural sector

Item Type	Thesis
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UNIVERSITY of LIMERICK

O L L S C O I L L U I M N I G H

The Design and Implementation of Animal
Auto Identification Systems for Application
within the Agricultural Sector

Submitted to

Department of Electronic and Computer Engineering
Faculty of Science and Engineering
University of Limerick

For the Degree of
Doctor of Philosophy

by

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Submitted to University of Limerick,

November 2012.

Abstract

Electronic systems in the agriculture industry are undergoing constant innovation. Within the dairy sector a large emphasis has been put on the development of automated milking parlours. These parlours are highly technological integrated mechatronic systems which have automated the processes of animal drafting, milk extraction and Cleaning-In-Place (CIP). This has led to efficient, high yielding farms with low operational costs. A vital component of these systems is the animal automatic identification (Auto-ID) system. Animal Auto-ID tags can be applied to the animal both internally and externally and allow for the contactless, electronic identification of animals as they enter, and through-out the milking parlour. This in turn allows the automation of the processes of cattle drafting, yield monitoring, animal weighting and feeding.

With the increase in the number of electronic systems in place both on and off farm, the milking parlour has become a far more hostile electromagnetic environment. This can have severe effects on the operation on an animal Auto-ID system, resulting in missed Auto-ID 'reads', which greatly affect the operation of the automated milking parlour, resulting in lower farm efficiency. In farms with integrated herd management systems and automated animal health monitoring systems, such problems can greatly affect both herd health and overall farm yield.

This research project was supported by Dairymaster® who are a world leader in dairy equipment manufacture. Dairymaster® identified a number of issues with their current Auto-ID system which they wanted to investigate. The main objective of this project examines the operation of current animal Auto-ID systems in the dairy sector and, through the use of a number of novel system designs, proves how current performance issues can be addressed. The final design increases the reliability of the Auto-ID system operation by decreasing the susceptibility of the system to electromagnetic interference (EMI). This was achieved by the development of a number of low-cost solutions to address the current systems performance and the redesigning of elements within the system such as; the Auto-ID reader, Antenna tuning system, the development of an EMI analysis tool and a digitally controlled power supply. This thesis also presents the development of a novel Digital Signal Processing (DSP) based Animal Auto-ID reader, including DSP algorithms, for the filtering and demodulation of an animal Auto-ID signals in the presence of strong EMI. A novel scheme for on-farm animal identification numbering is also outlined, which will aid the operation of animal Auto-ID systems in areas of high EMI.

Five case studies are presented which describe the advancements made in the area of animal Auto-ID systems, as a result of the work carried out. Each case study has been written in a style which allows each to be taken in isolation or as part of the greater body of work. The work has been of major benefit to the collaborating company and as a direct result will allow them to sell their Auto-ID system into markets that are prone to EMI and were of major concern.

This project has been undertaken through the Irish Research Council for Science, Engineering & Technology (IRCSET) Enterprise Partnership Scheme, in collaboration with an industrial partner, Dairymaster®.

Declaration

This thesis is presented in partial fulfilment of the requirements of the degree of Doctor of Philosophy.

It is entirely my own work and has not been submitted to any other higher education authority or for any other academic awards in the University.

Where there has been use made of the work of others, it has been fully acknowledged and referenced.

Mo bhuichas daoibh

Daniel Riordan

November, 2012

Acknowledgements

I would firstly like to thank Dr. Joseph Walsh, my principle supervisor on this project. He has helped me greatly during this project and, hopefully, many future projects. I would also like to thank my supervisors, Dr. Edmond Harty of Dairymaster[®] and Dr. Ian Grout of The University of Limerick. They have given me much support and advice throughout this project.

Funding has been granted for this project under the IRCSET Enterprise Partnership Scheme. This funding has been provided in conjunction with an industrial partner, Dairymaster[®]. I am very grateful for the trust these bodies have put in me to carry out this work.

I must also thank my family, friends and, especially my wife, Maria, for their constant support throughout this research project.

Due to the collaboration of an industrial partner, the content of this thesis is confidential and, therefore, an access embargo has been requested for a period of five years from thesis submission.

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List of Abbreviations

3gpp	3rd Generation Partnership Project
ADC	Analogue-To-Digital Convertor
ALU	Arithmetic Logic Unit
AM	Amplitude Modulation
ASIC	Application Specific Integrated Circuit
ASK	Amplitude Shift Key
Auto-ID	Automatic Identification
BER	Bit Error Rate
BSE	Bovine Spongiform Encephalopathy
CIP	Cleaning-In-Place
CISC	Complex Instruction Set Computer
COS	Commercial Off-the-Shelf
CPLD	Complex Programmable Logic Device
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
DAC	Digital-to-Analogue Convertor
DCM	Digital Clock Manager
DSP	Digital Signal Processing
DSP	Digital Signal Processor
EDA	Electronic Design Automation
EDIF	Electronic Design Interchange Format
EEPROM	Electrically Erasable Programmable Read Only Memory
EM	Electromagnetic
EMI	Electromagnetic Interference
EPROM	Erasable Programmable Read Only Memory
EU	European Union
FDX	Full Duplex
FDX-ADV	Full Duplex Advanced
FIPO	Field Instantly Programmable Oscillators

FIR	Finite Impulse Response
FPGA	Field Programmable Gate Array
FSK	Frequency Shift Key
HDL	Hardware Description Language
HDX	Half Duplex
HDX-ADV	Half Duplex Advanced
HF	High Frequency
IC	Integrated Circuit
IIR	Infinite Impulse Response
IP	Intellectual Property
IRCSET	Irish Research Council for Science, Engineering & Technology
ISM	Industrial, Scientific, and Medical
ISO	International Standardisation Organisation
ITU	International Telecommunications Union
ITU-R	International Telecommunications Union – Radio Communications
JEDEC	Joint Electron Device Engineering Council
JTAG	Joint Test Action Group
LED	Light Emitting Diode
LF	Low Frequency
LSB	Least Significant Bit
MAS	Multiply-Accumulate Operator
MCU	Microcontroller Unit
MIPS	Million Instructions Per Second
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor
MSB	Most Significant Bit
NAP	National Access Program
PCB	Printed Circuit Board
PGA	Pin Grid Array
PGA	Programmable Gain Amplifier
PLD	Programmable Logic Device
PROM	Programmable Read Only Memory
PSK	Phase Shift Key
RAM	Random Access Memory

RF	Radio Frequency
RFID	Radio Frequency Identification
RISC	Reduced Instruction Set Computer
RLC	Resistance-Inductance-Capacitance
SAR	Successive-Approximation Register
SMT	Surface Mount Technology
SoC	System-on-a-Chip
SOS	Second Order System
SPLD	Simple Programmable Logic Device
SPS	Samples Per Second
UART	Universal Asynchronous Receiver/Transmitter
UHF	Ultra High Frequency
VHDL	VHSIC hardware description language

Chapter 1

Introduction

1.1 Project Motivation

The current requirement for increased global traceability of animals and animal food products has driven the introduction of mandatory trace-back systems in the European Union (EU) [1] and countries such as New Zealand [2], Canada [3] and Japan [4]. This has led to the use of Radio Frequency Identification (RFID) based animal Automatic Identification (Auto-ID) systems in many livestock facilities. In Canada and some areas of Australia these trace-back systems have become mandatory once the animal has left the herd of origin [3, 5]. Such Auto-ID systems are often not only used on a national and global scale for food product traceability, but also on an on-farm scale as an integral part of an automated precision agricultural management system.

In recent years the development of automated milking parlours has been identified as a method of alleviating the manual labour involved in milking cattle. Many dairy farmers now operate semi or fully automated parlours incorporating Auto-ID systems, powered gates, teat spraying systems, automatic feeders, Cleaning-In-Place (CIP) and herd management software. Many of these milking parlours have now almost entirely automated the milk extraction process.

With this level of automation, milking parlours are becoming far more complex environments, requiring more advanced electronic system control for the operation of devices such as motors, pumps, solenoids and actuators, each requiring a range of sensor inputs for correct operation. The problem lies with milking parlours becoming increasingly more hostile electromagnetic (EM) environments, due in part to the presence of increased levels electronic equipment, with the addition of external factors. This is of major concern as the operation of the automated milking parlour is becoming increasingly reliant on the use of Auto-ID systems.

Animal Auto-ID systems used in agriculture operate in the Low Frequency (LF) band, in accordance with International Standardisation Organisation (ISO) [6] standards. These systems use a network of readers and passive (battery-less) electronic animal tags for the efficient identification, drafting and tracing of animals within the parlour. As passive tags do not have their own power source, power must be scavenged wirelessly from the Auto-ID reader activation field in order to transmit their stored ID information. This leads to a low energy level being available to the tag for data transmission, which in turn leads to a very low intensity signal being transmitted. With the reception of such a low-level signal being the cornerstone on which animal Auto-ID is based, the presence of electromagnetic interference (EMI) represents a serious problem which regularly affects the operation of Auto-ID systems. This creates large problems in the efficient operation of an automated milking parlour.

1.2 Industrial Partner and Project Funding

Dairymaster[®] [7] is an Irish company who have become one of the world's leading dairy farm equipment manufacturers, specialising in automated milking parlours. Dairymaster[®] have developed, in-house, a number of electronic systems for use in the automation of dairy parlours. These systems include animal Auto-ID systems, automatic cattle drafting and feeding, teat spraying, cluster removal and heat detection systems which have combined to almost entirely automate the milk extraction and herd management process. This project has been undertaken through the Irish Research Council for Science, Engineering & Technology (IRCSET) Enterprise Partnership Scheme [8], in collaboration with Dairymaster[®]. With the aid of Dairymaster[®], this project has undertaken an investigation into animal Auto-ID systems as used in an automated dairy parlour.

1.3 Aims of Project

The main aim of this project was to examine the current state of the art in animal Auto-ID systems in an agricultural setting and identify techniques which will yield a greater level of reliability and automation for these systems. The main result of this project was the development of an animal Auto-ID system which can operate in the

presence of the EMI found in an agricultural setting. In addition to this, several other issues involving the operation of an animal Auto-ID system were identified and analysed.

Project Objectives:

- To develop a device to facilitate the automatic self-tuning of an animal Auto-ID reader antenna circuit.
- To develop a prototype, low-cost animal Auto-ID reader, complying with International Standards Organisation (ISO) Animal Auto-ID standard, using Commercial-Off-the-Shelf (COS) components, which will have an equal or higher performance to the current industry standard.
- Examination of the effects of EMI on the performance of Animal Auto-ID systems.
- Investigation of the use of digital signal capture of the backscattered Auto-ID tag signal and Digital Signal Processing (DSP) to reduce the effects of EMI on Auto-ID system performance
- Development of a Field Programmable Gate Array (FPGA) based animal Auto-ID reader incorporating advanced DSP-based algorithms for the interrogation of animal Auto-ID tags in the presence of strong EMI.
- Development of a novel animal Auto-ID animal ID numbering system which will aid in electronic animal identification in the presence of EMI.

1.4 Novel Contribution of Work

This thesis makes two distinct novel contributions to the current state-of-the-art of animal Auto-ID. These contributions are presented in detail in Case Study 4 and Case Study 5 of this thesis.

1. A marked advancement in the area of EMI mitigation for the purpose of animal Auto-ID is presented which incorporates frequency band power monitoring, a novel intelligent digital filtering system and interference based signal demodulation. A DSP-based system on-FPGA is presented for the demodulation of Frequency Shift Key (FSK) in the presence of EMI of the type encountered on-farm. This project identified the characteristics of EMI

present on-farm and developed a novel specialised algorithm to allow animal Auto-ID systems to operate with greater reliability in these environments. The use of frequency band power monitoring has allowed the system to automatically identify the characteristics of the EMI present and adjusts the FPGA configuration accordingly to achieve more reliable Auto-ID tag interrogation.

2. In addition to this, a novel multi-interrogation based method for Auto-ID tag data identification in the presence of intermittent EMI is presented. It is shown that by amalgamating the resulting bit-streams of a series of failed tag reads, the correct tag ID number can be determined, with a specified confidence associated with each bit. During additional bit-error analysis of received tag IDs, a distinct pattern was identified in the tag-read errors occurring in the presence of consistent EMI signals. It was found that, statistically, the Cyclic Redundancy Check (CRC) error detection routine used in standardised animal Auto-ID tags is more likely to be received in error than any other section of the transmitted ID code, resulting in a failed, or ‘missed’, read. To allow greater reliability of animal Auto-ID, a novel system of on-farm animal identification numbering was devised, which can be used within a confidence based demodulation and decoding routine.

1.5 Thesis Structure

This thesis will begin with a literature review covering the current state of the art in the field of animal Auto-ID systems as used in an agricultural setting, particularly focusing on the dairy industry. This review is divided into three chapters, the first focusing on RFID systems, the second on RFID in the context of animal Auto-ID and the standardisation of Animal Auto-ID systems. A final literature review chapter describes the components of an agricultural electronic embedded system.

Five case studies are presented which describe the work carried out in the area of animal Auto-ID systems. Each case study has been written in a style which allows each to be taken in isolation or as part of the greater body of work. While the novel

content of the work is contained in the final two case studies, three preceding case studies are also presented as the outcomes from each case study make a distinct improvement to the overall operation of animal Auto-ID systems as used in the dairy sector. Each case study examines a particular aspect of animal Auto-ID system operation, which is illustrated in figure 1.1.

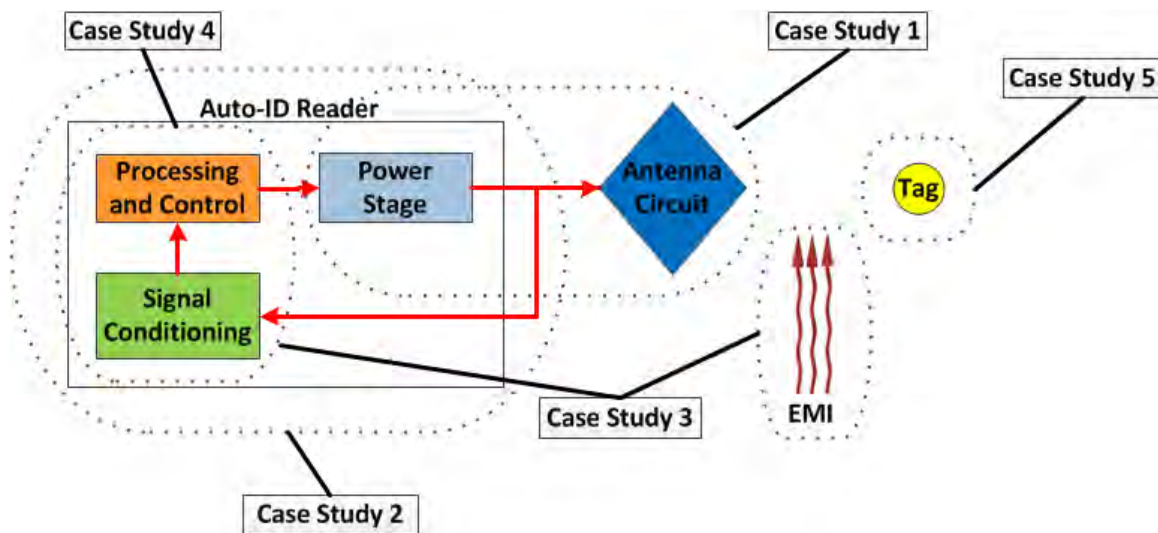


Figure 1.1: Auto-ID System Block Diagram and Thesis Structure

Case study 1 describes the development of a system for the automatic tuning of the antenna circuit and automatic read-range adjustment of an animal Auto-ID reader. Through the use of antenna voltage monitoring, an inductive-capacitive antenna circuit is tuned to resonance, while the Auto-ID system read-range is adjusted through the use of a low-cost digitally controlled power supply with the capability of providing the high current required for the operation of an animal Auto-ID system.

A current limitation to the introduction of animal Auto-ID systems in an automated dairy parlour is the high cost of animal Auto-ID readers. Case Study 2 documents the development of a low-cost animal Auto-ID reader based around an off-the-shelf base-station integrated circuit (IC). This reader will be a direct low-cost alternative to the current animal Auto-ID reader module in use by this project's industrial partner.

EMI has long been a problem in the operation of wireless communications, including animal Auto-ID systems. Case Study 3 presents the development of a low-

cost system for the reception, storage and digital analysis of EMI in an agricultural setting. This system allows the analysis of existing EMI in the field to allow informed system development and installation. Also presented in this case study is the development of a prototype bench-top DSP-based animal Auto-ID reader capable of implementing extremely powerful digital filtering on the received Auto-ID tag signals.

With the concept of a DSP-based animal Auto-ID reader proven in Case Study 3, along with the characterisation of on-farm EMI, a more powerful DSP-based system is developed in Case Study 4. This system is constructed around an FPGA, allowing development of novel DSP algorithms for the filtering and demodulation of animal Auto-ID signals in the presence of strong EMI of varying types.

Examination of Bit-Error Rates (BER) in the reception of animal Auto-ID codes led to the identification of a number of interesting bit error patterns. Case Study 5 makes use of the identified error patterns in the development of a novel, more robust animal identification numbering scheme and multi-read interrogation technique for use on-farm.

This thesis ends with a conclusion discussing the project outcomes, detailing the major contributions made to the state-of-the-art. Opportunities for further research are also discussed.

1.6 References

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Chapter 2

An Overview of Radio Frequency Identification and Programmable Logic Technologies

Radio Frequency Identification (RFID) is a method which is currently employed, and continually researched, for the purpose of Automatic Identification (Auto-ID). RFID technology can be used to locate, track, analyse and uniquely identify inventory using electronic tags and wireless readers. In recent years RFID technology has become a major player in the Auto-ID sector and threatens to overtake many more established Auto-ID technologies in supply chain management, such as bar-code product identification.

Generally, an RFID system consists of three components; a series of RFID tags, an RFID reader (or interrogator) and a PC hosting software to control the reader and track the tagged items. A typical RFID system is shown in figure 2.1. RFID tags are relatively small portable devices composed of an integrated circuit (IC) connected to a Radio Frequency (RF) interface. Modern RFID ICs contain sizable memory locations which can hold a significant amount of digital information. These stored data are then accessible using an RFID reader via the RF interface.

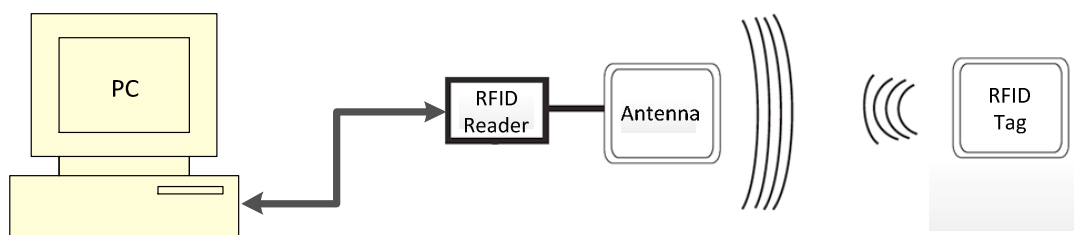


Figure 2.1: RFID System

An RFID reader consists of an RF interface, a limited amount of data processing hardware and a communications interface which often integrates to a PC. The information stored in RFID tag's memory can be accessed by the reader via the RF interface if the tag is positioned within the interrogation zone of the reader. These data

are then either processed within the RFID reader (for simple applications) or transferred to the PC running supply chain management software.

There are many types of RFID tags and readers currently available with numerous capabilities and features, allowing for a range of possible applications to suit particular product categories. The general concept of RFID is not a new technology. It has been used in various forms since World War II, when Allied aircraft were fitted with electronic transponders to alleviate the possibility of friendly fire. In recent years major advancements have enabled the use of RFID for Auto-ID requirements in a product supply chain, and have given RFID the potential to overtake and replace existing technologies.

This chapter will present an overview of RFID technology to allow greater understanding of RFID-based animal Auto-ID systems, the primary focus of this thesis. Beginning with a short history of RFID technology, the chapter will then proceed to describe the operation of the technology, addressing features such as; frequency of operation, tag power supply, tag communication and standardisation and an overview of the current applications of the technology.

This chapter will conclude with a description of Programmable Logic Devices (PLDs), which are employed in this thesis for the development of an advanced animal Auto-ID reader.

2.1 History of RFID Technology

RFID technology has its roots in World War II, when the Allied Air Force used a system of reflected energy to distinguish between friendly and enemy aircraft. After the war, these advances were built upon by such early research as “Communication by Means of Reflected Power” [1]. At this time RFID-style systems were hugely expensive and therefore the idea of RFID as an efficient method of Auto-ID was not investigated.

The 1960s and 70s saw a renewed interest in the technology of “reflected power” with the development of basic passive transponder based systems by Richardson and Vinding. 1975 saw a major step forward in RFID technology with the development of the technique of antenna load modulation for the efficient transmission of data from a passive transponder. [2]

With the reduction in system cost through the use of semiconductor technology, the 1990s saw the implementation of large-scale RFID-based inventory management and automation systems, such as electronic ticketing and animal tracking. Further reductions in the cost of RFID tags and increased standardisation has allowed major industrial groups, such as Wal-Mart[®], to introduce RFID-based inventory management systems and to mandate the use of such systems for their suppliers.

2.2 RFID Technology

RFID is a contactless identification technology which uses Radio Frequency (RF) Electromagnetic (EM) signals for the querying of electronic ID tags and the subsequent transmission of the ID information stored on the tag. The basic concept of RFID is that by attaching an RFID tag to an item, an automated inventory system can track that item without human intervention. If a user has the ability to track an item through key events in its ‘life’, the process flow through the supply chain can be automated.

The main features which differentiate various RFID technologies are; operating frequency, tag power supply and communication protocol.

2.2.1 Operating Frequency

RFID systems operate over a wide frequency range from 125 kHz (Low Frequency) to 5.8 GHz (Microwave). The choice of operating frequency has a fundamental effect on the design, operation and capabilities of an RFID system. As RFID systems operate through the use of EM waves, they are subject to the properties governing EM-fields and EM-wave propagation which are largely frequency dependent. For example, the absorption rate of a metal, water and non-conductive

materials with high dielectric constants is inversely proportional to frequency. Therefore low-frequency (LF) RFID systems are more suitable for operation in environments where such materials are prominent. On the other-hand, high-frequency (HF) systems tend to have longer read-ranges. [2]

It must also be noted that, as RFID systems transmit information through the use of EM waves, they are classified as radio transmitters. The operation of a radio transmitter requires a licence in most jurisdictions unless it is operating at a frequency within one of the Industrial, Scientific and Medical (ISM) frequency bands. Operation of a RFID system outside of the ISM bands may cause interference with a licensed radio communication system.

Frequency range	Centre frequency	Availability
6.765–6.795 MHz	6.780 MHz	Note 1
13.553–13.567 MHz	13.560 MHz	
26.957–27.283 MHz	27.120 MHz	
40.66–40.70 MHz	40.68 MHz	
433.05–434.79 MHz	433.92 MHz	Region 1 only (Note 2)
902–928 MHz	915 MHz	Region 2 only (Note 2)
2.400–2.500 GHz	2.450 GHz	
5.725–5.875 GHz	5.800 GHz	
24–24.25 GHz	24.125 GHz	
61–61.5 GHz	61.25 GHz	Note 1
122–123 GHz	122.5 GHz	Note 1
244–246 GHz	245 GHz	Note 1

Table 2.1: The ISM Frequency Bands [3]

Note 1: Subject to local national radio regulations

Note 2: Region 1: Europe, Africa, the Middle East west of the Persian Gulf including Iraq, the former Soviet Union and Mongolia. Region 2: Americas and the Eastern Pacific

The ISM frequency bands were originally reserved for use within the fields indicated in the title and detailed in Table 2.1. Confining the operation of unlicensed devices to the ISM frequency bands allowed for licensed communication systems to operate outside of these frequency bands (in licensed communications bands) without interference from these devices. The EM spectrum is regulated by the International Telecommunications Union – Radio Communications Sector (ITU-R), who defines

the ISM frequency bands in article 5 of their ‘Radio Regulations’ [3]. Many error tolerant communication systems, such as wireless headsets, intercoms and RFID, use the ISM frequency bands as it allows operation without a radio license. In addition to these frequency bands, all frequencies below 135 kHz are available for use. [4]

LF RFID systems operate in the unregulated band below 135 kHz. These systems, such as animal Auto-ID and access control systems, operate in the near-field EM region and therefore range is limited by the near/far-field EM boundary. For the commonly used frequencies in the region of 130 kHz the boundary limit is approximately 372 m, as given by equation 2.1, where λ is the wavelength of the frequency of operation. In addition to this, the high loss factor of EM-field strength in the near field gives LF tags a low read-range. These factors are described in greater detail in section 2.2.2.

$$D = \lambda / 2\pi = c / 2\pi f \quad (2.1)$$

Where,

c = speed of light (m/s)

D = near/far-field boundary limit (m)

λ = wavelength (m)

f = frequency (Hz)

HF RFID systems, often operating at a frequency of 13.56 MHz, generally use the principle of near-field coupling for data transmission. As the near-field boundary is inversely proportional to the frequency of operation, the boundary at 13.56 MHz is reduced to 3.5 m. Therefore the read-range of 13.56 MHz is greatly reduced with respect to that of LF systems. The HF frequency range is often used for RFID based access control and smart ticketing systems, which generally require low-power systems with shorter read-ranges.

Systems operating in the Ultra-High-Frequency (UHF) range of 860 – 960 MHz have become the leading technology in RFID-based supply chain management and electronic toll collection over the past decade. These systems are characterised by the

requirement for long-range and high-speed tag interrogations, using far-field coupling. Many UHF RFID systems have read ranges in excess of 3 m, with some active systems claiming ranges of up to 30 m. Many UHF systems have encountered difficulties in the interrogation of tagged items containing liquids or metals. [5]

Microwave RFID systems operate at a frequency of 2.45 GHz predominantly using far-field coupling. Due to their high frequency of operation they have both a high data transmission rate and a large read-range of approximately 30 m. On the downside, microwave RFID tags have higher power consumption and are more expensive than other tag types. [6]

2.2.2 Tag Power Supply: Active, Semi-Passive or Passive

RFID systems are often categorised based on the method by which the systems RFID tags are powered. A system containing battery powered tags is referred to as an active system, while a system in which the tags do not contain their own power source is known as passive. Passive tags must harvest all of their energy from the EM activation field emitted by the reader. Semi-Passive tags use an on-board battery to operate the tag circuitry, such as processors, memory and sensors, but harvest the energy for use in data transmission from the EM-field emitted by the reader.

RFID tags consume extremely low levels of power, in the order of $10 \mu\text{W}$ to 1 mW per interrogation [7]. Such low power consumption is required for both active and passive tags as both operate under severe energy limitations. While active tags contain their own power source, the life-time of these tags is limited by the amount of energy stored in the battery. Therefore, if a reasonably long lifetime is required, power consumption must be low. A visual comparison of Active and Passive RFID tags is presented in figure 2.2.

Active Tags

Active tags contain their own power supply, usually in the form of a battery. The requirement for an on-board power source that will serve the life-time of the tag make active RFID tags larger and more costly than passive tags. Upon reception of an interrogation signal from a tag reader, an active tag will transmit its response containing its ID information. This response is powered directly from the tag's own

power source. Certain active tags are designed to constantly transmit their ID information. These tags require even larger battery power supplies and therefore are larger and more expensive than intermittently transmitting active tags.

Passive tags

Having no power supply of their own, passive RFID tags operate by harvesting energy from the RFID readers’ activation field. Passive RFID systems achieve this energy transfer through two distinct methods; the inductive (magnetic) coupling of the reader antenna with the tag antenna and EM-wave capture, often referred to as radiative coupling.

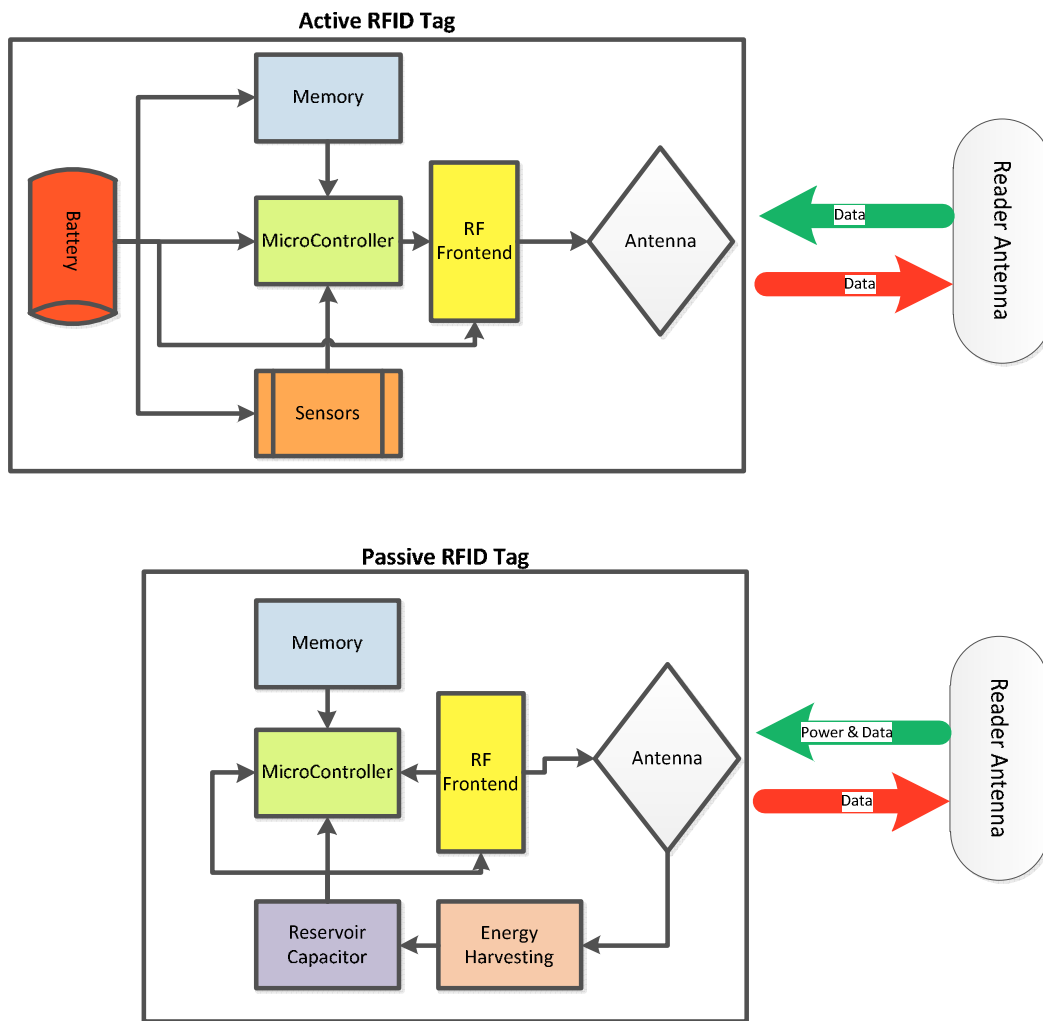


Figure 2.2: The Operation of Active and Passive RFID Tags

The predominant method used by a system is based on the field of operation of the system. The field of operation is divided into two regions, ‘near-field’ and ‘far-field’. The boundary between the two is defined in equation 2.1. This boundary is not a

distinct boundary, and much overlap between the two regions may occur. Within the field boundary, the EM-field created by the reader antenna consists of stored energy which is still strongly bound to the antenna. Beyond the boundary the EM-field begins to decouple from the antenna and become a separate EM wave.

The near/far-field boundary of a given RFID system is inversely proportional to its frequency of operation. For this reason, LF to HF systems are generally designed to operate in the near-field region, while UHF and microwave based RFID tags are designed to operate in the far-field, to provide a usable system range. The antenna circuits of some tags (usually HF) may be designed to utilise both near and far-field energy transfer.

Inductive coupling is the dominant form of energy transfer in the near-field region. When a current is present in a conductor, a magnetic field is generated around that conductor. Similarly, when a conductor is present in a magnetic field, a current is generated within the conductor. This is known as inductive coupling. Many LF and HF RFID tags utilise this phenomenon to harvest power from the magnetic field created by the RFID reader. Within the near-field region EM-field strength is inversely proportional to the cube of the distance from the antenna, effectively limiting a system's read-range to shorter distances. [8]

Radiative coupling energy transfer is predominant in the far-field region. Here the energy is harnessed through the potential difference generated on the tag antenna due to the presence of an EM-wave. In the far-field region the degradation of the EM field strength is proportional to the inverse-square of the distance, allowing far-field RFID tags to operate at greater distances. [8]

Semi-Passive Tags

Semi-Passive Tags are often used when a certain amount of data acquisition and storage is required when the tag is not within an interrogation zone. During this time any sensors and memory in operation are powered by the tag battery. Then the tag enters an interrogation zone, the power harvested from the reader activation field is used to transmit the data to the reader.

2.2.3 Data Transmission

Once an RFID tag is activated, the data stored on the tag must be transferred back to the reader device using some means of RF interface. This interface is generally achieved in one of two ways, depending on whether near-field or far-field coupling is employed. These coupling regimes are similar to the methods of energy transfer outlined in section 2.2.2.

The data stored on the tags must be modulated onto a carrier waveform in order to be successfully transmitted to the reader system. RFID systems predominantly use three modulation techniques, Amplitude Shift Keying, Frequency Shift Keying and Phase Shift Keying. A comparison of these three modulation schemes can be seen in figure 2.3.

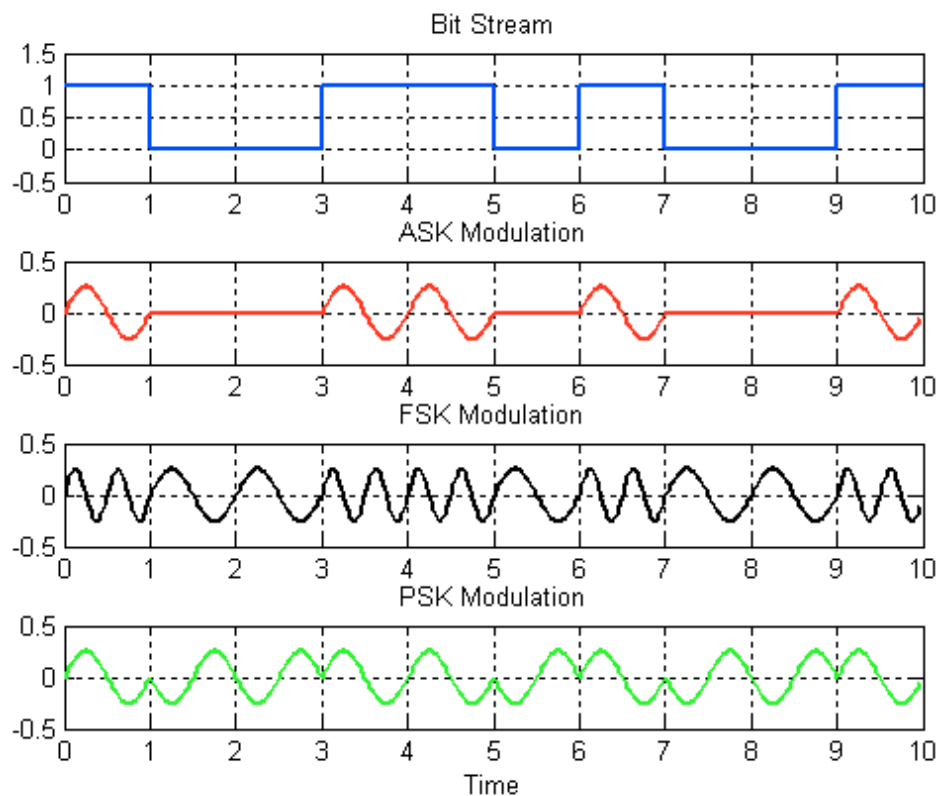


Figure 2.3: ASK, FSK and PSK Modulation

Amplitude Shift Keying (ASK) is a modulation technique in which the digital data to be transmitted is modulated on the carrier wave by means of varying the amplitude of the carrier between two discrete levels. In the near-field region ASK transmissions are often accomplished through the load modulation technique. [9]

Frequency Shift Keying (FSK) is a modulation method in which digital information to be transmitted is represented by changes in the frequency of the carrier signal. FSK differs from frequency modulation (FM) in that FSK uses only two discrete frequencies, as only two discrete values, '1' and '0', need to be represented in the modulation scheme. [10]

Phase Shift Keying (PSK) is a modulation technique which uses variations in the phase of the carrier wave to represent digital data to be transmitted. The most popular and robust PSK scheme uses two phases separated by 180° to represent either a binary '1' or '0'. [11]

2.3 Applications of RFID

In the last number of decades RFID technology has found applications in many fields including inventory management, access control, E-ticketing, industrial automation, animal identification and medical applications. It has been found that the correct choice of RFID technology to be used within an Auto-ID system is highly dependent on the system's application. Included in the technological description of RFID systems presented in section 2.2 are the advantages and limitations of each aspect of different RFID systems. Based on these parameters a suitable RFID technology can be chosen for a specific application.

To date the most high-profile use of RFID has been that of Wal-Mart[®] who in 2005 made the use of RFID technology mandatory for their inventory management system. Wal-Mart[®] also made it compulsory for many of their largest suppliers to ensure that their products were RFID enabled [5]. Other high profile RFID implementations include the US Department of Defense requirement for their suppliers to ensure their products are RFID enabled and the worldwide use of RFID technology in toll-collection systems such as toll-motorways and automatic transport fare collection. [2]

Contactless ‘Smart Cards’ are used as a means of payment in many public transport systems, such as the Octopus Card in Hong Kong [12], the Oyster Card in London (figure 2.4) [13] and the Leap Card in Dublin, Ireland [14], to name but a few. Recently, more advanced contactless payment systems using RFID technology have been developed. MasterCard®’s PayPass RFID enabled credit cards allow for ‘Tap&Go’ payment, significantly streamlining the purchasing of smaller goods. [15]

Since 2009, DeviceFidelity®, in conjunction with a number of credit card companies, have developed specialized devices, with the form factor of a MicroSD card, which can act as both an RFID reader and passive RFID tag. Once inserted into the MicroSD slot of certain mobile phones, the device can connect directly to a bank account via the GSM/3G network, enabling mobile payments. [16]



Figure 2.4: London’s Oyster Card in Use on Public Transportation [12]

RFID systems are also widely used in asset management and inventory systems, where individual items are tagged with RFID tags to allow easy contactless identification and data entry. In many cases handheld readers are used to interrogate the RFID tags and wirelessly transmit the tag information to a PC operating asset management software. In other cases portal style readers are placed at the entry and exit points of warehouses to monitor the movement of assets in and out of the facility, again with the aid of asset management software.

From the mid-2000s onwards RFID enabled e-passports have become standard in many countries throughout the world, with the US mandating their use for countries

operating under their Visa Waver Program. The RFID IC embedded in each International Civil Aviation Organization (ICAO) standardised e-passport must contain all data held on the data page of the passport, including the photograph. [17]

In certain instances, RFID has been used as a personal identification device, implanted into humans. This is generally carried out by choice to allow increased automation of tasks such as home entry, PC login, storing medical records for emergency use and activity monitoring. [18]

This thesis will focus on RFID systems which are used for the automatic identification of animals. This application of Auto-ID technology is covered in detail in chapter 3.

2.4 Sensor Enabled RFID

In recent years, advances in the development of low-power sensors have allowed the integration of sensors into RFID tags. Sensors were initially employed in active tags due to the power requirements of sensor operation. The advent of low power sensors has allowed their integration into passive RFID tags.

The key to the current success of sensor-enabled tags is their ability to operate using only the power harvested by the tag antenna circuit. This allows the sensor to operate without maintenance, but can only operate when power harvested from the reader is available [19]. Other sensors-enabled RFID tags have their own battery power source which enables them to operate their sensing function continuously and transmit all their stored data when interrogated [7]. The life span of these sensors is limited by the lifetime of their battery and may require regular servicing to allow battery replacement. Sensor systems are often integrated with RF enabled memory ICs such as the STMicroelectronics[®] M24LR64 [20]. These ICs have dual communication interfaces, with a wired interface to communicate with the sensors and an RFID style RF interface for wireless communications.

2.5 Overview of Programmable Logic Technology

Within embedded electronics there are two fundamental methods for performing computation, hardware and software. Hardware computation is often implemented in an Application Specific Integrated Circuit (ASIC) and is used for highly critical and high-speed computation. ASICs provide an elegant, low-power and high-performance solution to computational problems, but their development comes at a high cost, both in terms of development time and manufacture. Once large scale production is achieved, ASICs become more affordable through economies of scale.

Software-based computation, which takes the form of a software program operating on a hardware processor, allows faster development time and a flexibility which permits alteration of the computation algorithm after implementation. Software provides a computational system which is easily reconfigured but with lower computational speed, high power consumption and using much greater areas of silicon than ASIC-based hardware computation. As all but the most advanced software-based computation can be implemented using off-the-shelf processor hardware, this method can often be produced at a lower cost than equivalent hardware-based computation.

Programmable Logic provides an excellent trade-off between the two techniques. It has the advantages of the quick development and prototyping of a software based system, while maintaining the power, silicon area and performance benefits of a purely hardware computation. Since their advent in the late seventies, Programmable Logic Devices (PLDs) have been one of the largest growing sectors in the semiconductor industry, with gate densities currently doubling every 18 months [25]. Meanwhile, the price of PLD ICs is dropping. In modern embedded electronic systems, re-configurable ICs such as the Simple Programmable Logic Device (SPLD), the Complex Programmable Logic Device (CPLD) and the Field Programmable Gate Array (FPGA) have been identified as a means of providing the ability to prototype and easily modify hardware functionality. The ability to program/configure hardware functionality post fabrication, and in the final application, is increasingly important for higher complexity devices, where increasing levels of flexibility are required. Today, in a single device, a designer can utilise high performance logic, memory, high-speed I/Os and heavy-duty signal processing with embedded processors. This

gives an electronic systems designer a significant productivity advantage when designing an electronic system.

Vendor	FPGA	CPLD	SPLD
Xilinx® [28]	SRAM Virtex 4, 5, 6, 7 Spartan, 3, 3A, 3AN, 3E, 6 Artix 7 Kintex7 EasyPath 7	FLASH CoolRunner II XACoolRunner II XC9500XL XA9500XL	
Altera® [29]	SRAM Stratix I, II, III, IV, V Cyclone I, II, III IV, V Arria I, II, V	EEPROM MAX 3000A, 7000 FLASH MAX II, IIG, IIZ, V	
Lattice Semiconductor® [30]	SRAM LatticeECP2/M LatticeECP3 LatticeECP4 LatticeSC/M LatticeXP2	EEPROM iCE 40 Series ispMACH 4000ZE Flash Mach XO, XO2	EEPROM GAL (Discontinued) PAL (Discontinued)
Texas Instruments® [31]			PROM PAL – High Performance Impact
MicroSemi® [32]	SRAM ProASIC3 Flash IGLOO		
Atmel® [33]	SRAM AT40K / AT40KAL	EEPROM ATF15xx Family ATF1508ASVL	EEPROM ATF16-22 Family ATF16V8B

Table 2.2: Main Programmable Logic Vendors and Device Summary

There are several devices currently available that can be used for advanced embedded electronic design, for example, the Xilinx® Virtex 5 FPGA [26] combines two PowerPC 440 cores, Data Conversion (Analogue to Digital and Digital to Analogue) with up to 5 million free gates, while the Stratix 5 from Altera® [27]

combines multi-Gigahertz transceivers with approximately the same number of free gates. The continued evolution of programmable technologies has enabled a single CPLD or FPGA to take the place of the entire traditional electronic system.

2.5.1 Types of Programmable Logic Architecture

The current range of PLDs include everything from small devices capable of implementing simple logic equations to huge FPGA's that can hold multiple processor cores, including extensive peripherals. In addition to this incredible difference in size there is also much variation in PLD architecture. A list of the top vendors, their products and a device summary is shown in table 2.2.

Simple Programmable Logic Devices (SPLDs)

At the lower end of the spectrum are the original PLDs. These were the first chips that could be used to implement a flexible digital logic design in hardware and are today referred to as Simple Programmable Logic Devices (SPLDs). SPLDs are often used as a direct replacement of a number logic element ICs within a circuit. If at a later time the simple logic equation needs to be changed, the SPLD can be quickly reconfigured without any other alteration to the circuit. Other names encountered for this class of device are:

- Programmable Logic Array (PLA),
- Programmable Array Logic (PAL),
- Generic Array Logic (GAL)

Early SPLDs were often used in address decoding, where they had several clear advantages over the 7400-series TTL parts which they replaced, such as requiring less board area and power than a series of ICs and the reconfigurable nature of the SPLD meaning that a change in the logic doesn't require any alteration to the Printed Circuit Board (PCB).

The building block of the PLD is the macrocell and inside each SPLD is a set of fully connected macrocells. These macrocells are typically comprised of some amount of combinatorial logic (AND and OR gates, for example) and a flip-flop, allowing a

small Boolean logic equation to be built within each macrocell. The particulars of the available logic gates and flip-flops are specific to each manufacturer and product family, but the general operation is always the same.

Complex Programmable Logic Devices (CPLDs)

As chip densities increased, it was a natural progression for the PLD manufacturers to evolve their products into larger (in terms of the number of logic element, but not necessarily physically) parts called Complex Programmable Logic Devices (CPLDs). For most practical purposes, CPLDs can be thought of as multiple SPLDs with programmable interconnects, within a single IC. The larger size of the CPLD allows the implementation of more complicated designs.

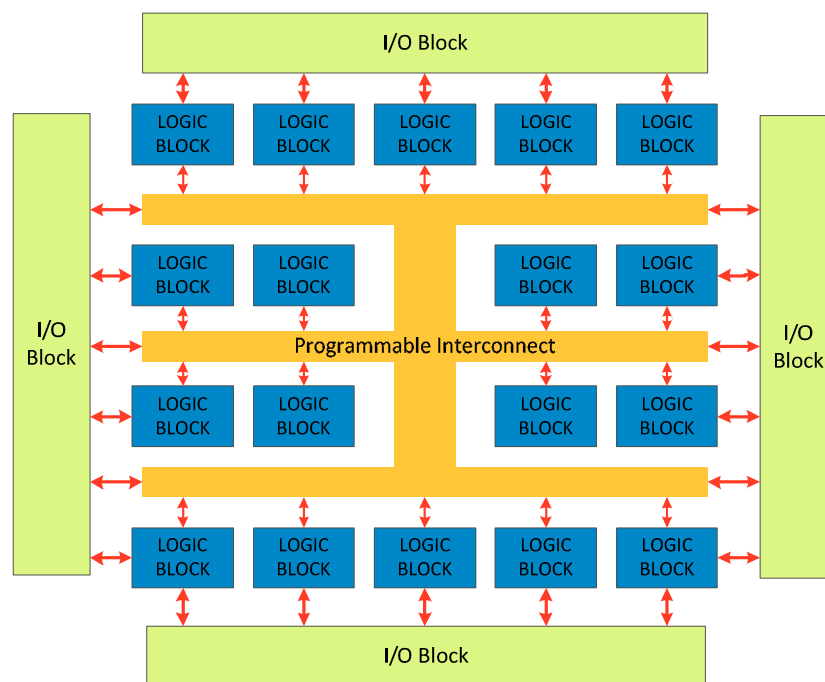


Figure 2.5: CPLD Internal Architecture

Figure 2.5 contains a block diagram of the internal architecture of a typical CPLD. Each of the logic blocks shown is the equivalent of one SPLD. These logic blocks are themselves comprised of macrocells and interconnect wiring. Unlike the programmable interconnect within a SPLD, the switch matrix within a CPLD may or may not be fully connected. Therefore, some of the theoretically possible connections between logic block outputs and inputs may not actually be supported within a given

CPLD. The effect of this is that it is often very difficult to make full utilization of the macrocells available.

CPLDs have found widespread use in the implementation of high-performance control-logic or complex finite state machines. At the higher-end (in terms of numbers of gates), there is also a degree of overlap in potential CPLD applications with FPGAs. Traditionally, CPLDs have been chosen over FPGAs whenever high-performance logic is required, as due its less flexible internal architecture, the delay through a CPLD (measured in nanoseconds) is more predictable and usually shorter.

Field Programmable Gate Arrays (FPGAs)

FPGAs can be used to implement almost any hardware design. They are commonly used to prototype a complex piece of hardware that will eventually be manufactured as an ASIC once the design has been verified. However, FPGAs are increasingly being used in the final product implementation, depending on the relative weights of development and production cost for a particular project. While the costs of ASIC development are significantly higher than that of FPGA system development, the cost per IC may be lower once ASIC manufacture has been ramped up to achieve economies of scale.

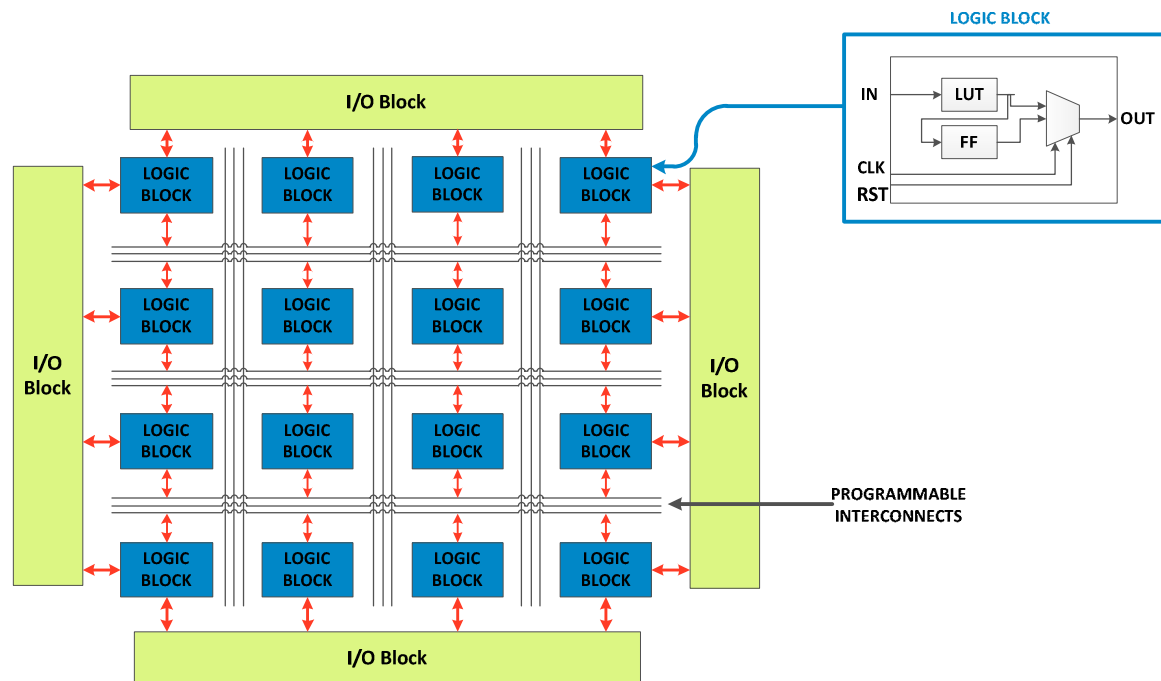


Figure 2.6: Internal Structure of a FPGA

The development of the FPGA was distinct from the SPLD/CPLD evolution just described. This is apparent when the internal structure of the FPGA is examined. Figure 2.6 illustrates a typical FPGA architecture. There are three key sections of its structure: logic blocks, interconnects, and I/O blocks. The I/O blocks form a ring around the outer edge of the FPGA. Each of these provides an individually selectable input, output, or bi-directional access to one of the general-purpose I/O pins on the exterior of the FPGA package. Inside the ring of I/O blocks lies a rectangular array of logic blocks. Connecting these logic blocks is the programmable interconnect wiring.

The logic blocks within an FPGA are small and simple when compared to the more complex macrocells of the SPLD/CPLD. The logic blocks of a CPLD contain multiple macrocells, while the logic blocks of an FPGA generally consist of a small number of logic gates, a look-up table and a flip-flop. It is the increase level of interconnects available between each logic block of an FPGA which allows a much more flexible architecture than that of a CPLD. This makes FPGAs more suited to register-heavy and pipelined applications. They are also often used in place of a processor-plus-software solution, particularly where the processing of input data streams must be performed at a very fast pace. In addition, FPGAs are usually denser (more gates in a given area) and cost less than comparable CPLDs, making them suitable for larger logic designs.

2.5.2 Hardware Design and Development

The process of creating digital logic is not unlike the embedded software development process. A description of the hardware's structure and behaviour is written in a high-level Hardware Description Language (HDL) (usually VHDL or Verilog-HDL) and that code is then synthesised and implemented to generate a configuration file for configuration of a PLD. Schematic capture is also an option for design entry, but has become less popular as designs have become more complex and the language-based tools have improved. The overall process of hardware development for programmable logic is shown in figure 2.7.

VHSIC hardware description language (VHDL) was originally developed in conjunction with the US Department of Defence to allow their logic IC suppliers to give detailed functional descriptions of the ICs they supplied. VHDL borrowed

heavily from the Ada programming language, a structured object-oriented high-level computer programming language which was in common usage within the US Department of Defense. VHDL was standardised by the IEEE in the standard IEEE1076-1987 [34].

Verilog-HDL, initially developed in the early 1980s, is a HDL similar in many ways to VHDL but with a distinct similarity to the C programming language. This has allowed an easier transition for many software programmers to begin the development of PLD-based devices. Verilog-HDL is standardised by the IEEE under standard IEEE 1364-1995 [35].

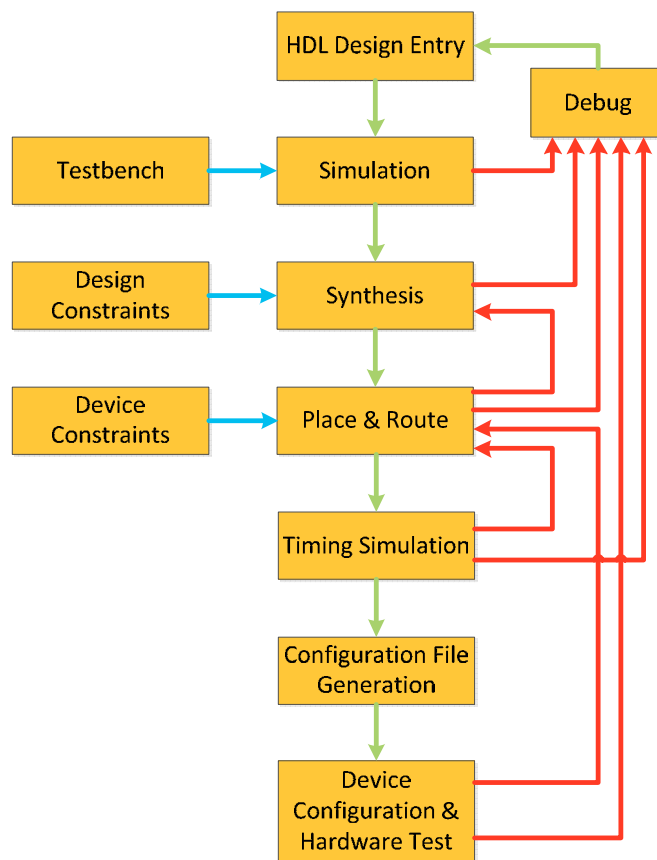


Figure 2.7: Programmable Logic Design Process

Perhaps the greatest difference between programmable hardware-based design and software-based design is how the system developer must approach the problem. Software development tends to progress sequentially, even when multithreaded applications are under development, while the hardware designer must consider the parallelism inherent in hardware implementation to ensure that the PLD is performing at its most efficient.

Typically, the design entry step is followed or interspersed with periods of functional simulation. A HDL simulator is used to execute the design and confirm that the correct outputs are produced for a given set of test inputs. Although further problems with the size or timing of the hardware may become apparent later in the design process, the designer can test the functionality of the design before proceeding on to the next stage of development. Design synthesis and implementation only begins after a functionally correct representation of the hardware exists.

This hardware compilation consists of two distinct steps. First, an intermediate representation of the hardware design is produced. This step is called synthesis and the result is a representation of the hardware design called a netlist. The generated netlist is independent of the specification of the target device. It is usually stored in a standard format called the Electronic Design Interchange Format (EDIF).

The second step in the translation process is often referred to as either ‘place & route’ or ‘implementation’. This step involves mapping the logical structures described in the netlist onto actual macrocells, interconnections, dedicated hardware structures and input and output pins within the PLD. This process is similar to the placing and routing of components and interconnects in the development of a PCB, and it allows for either automatic or manual layout optimisations techniques. The result of the ‘place & route’ process is a bit-stream. This name is used generically, despite the fact that each CPLD or FPGA (or device series) has its own bit-stream format. The most common bit-stream is a JEDEC (Joint Electron Device Engineering Council) format.

The ‘place & route’ process also generates a signal delay report, which indicates the internal hardware delays within the target PLD for the established interconnects, which may affect the functionality of the design. This delay report is used to perform the timing simulation step, which models the inherent hardware delays of the configured system and insures continued system functionality.

The JEDEC file contains the fuse map of the original logic design and is downloaded to the PLD programmer to configure the specified PLD [36]. This JEDEC bit-stream is the binary data that must be loaded into the FPGA or CPLD to

cause device to be configured to a particular hardware design. Increasingly, debuggers have become available which allow for single stepping the hardware design as it executes within in the PLD.

PLD EDA Toolsets

Most PLD vendors offer sophisticated Electronic Design Automation (EDA) tool suites which allow the designer to create complex digital designs and implement them on the vendors PLDs. These toolsets are commonly available by free download, or at an extremely low cost, directly from the device vendors, in order to entice new designers to use their devices [37, 38]. Some vendors offer their tools free-of-charge, but charge for support for their most expensive devices. Others offer limited capability toolset for free and charge for increased functionality.

While some PLD manufacturers have developed their EDA toolsets in-house, others partnered with EDA companies specializing in PLD synthesis to deliver robust solutions to their mutual customers. This has led to some PLD vendors offering proprietary synthesis tools as part of their low-cost (or free) tool suites while continuing to partner with commercial EDA companies for higher-end solutions. Others rely exclusively on their partnerships with commercial EDA companies for synthesis and offer customized versions of commercial EDA tools as part of their tool suite. The two largest PLD vendors, Xilinx[®] and Altera[®], both fall into the first group, offering internally developed synthesis tools as part of their suites, while Actel[®], and Lattice Semiconductor[®] offer special versions of EDA-supplied synthesis products.

As PLD applications grow both broader and more complex, PLD vendors have tackled problems beyond just synthesis, simulation, and place-and-route. To become a viable option for Digital Signal Processing (DSP), for example, they've been forced to tackle the task of developing design flows from algorithmic tools such as Mathworks[®] MATLAB[®] and Simulink[®] [39]. For embedded computing on PLDs, they've added platform assembly tools such as Xilinx[®] Platform Studio [40] and Altera Corporation[®] Nios II Embedded Design Suite [41]. In many cases, they've looked to partnerships with EDA companies to bolster their capabilities in these new areas.

2.5.3 PLD Configuration

Once a configuration bit-stream has been generated for a PLD by a logic synthesis tool, the user can configure the device in a number of ways, based upon the device technology. Many PLDs are similar to non-volatile memories as already discussed and may be based on Programmable Read Only Memory (PROM), Erasable Programmable Read Only Memory (EPROM), Electrically Erasable Programmable Read Only Memory (EEPROM), and Flash technology. Just like their memory counterparts, PROM and EPROM-based logic devices can only be programmed with the help of a separate piece of lab equipment called a device programmer. On the other hand, many of the devices based on EEPROM or Flash technology are in-circuit or in-system programmable (ISP). This makes it possible to erase and reprogram the device via a Joint Test Action Group (JTAG) standard interface [42] or from an on-board embedded processor.

In addition to non-volatile technologies, there are also PLDs based on Static Random Access Memory (SRAM) technology. In such cases, the configuration of the device is volatile meaning that the internal logic must be reloaded after every system or chip reset. Therefore an additional non-volatile memory device, external of the PLD, is required, from which the bit-stream can be loaded to the volatile PLD upon start-up. There is an advantage to this in that the configuration of the PLD can be manipulated ‘on-the-fly’ during system operation, with the requirement of a PC connection.

Partial Re-configuration

In much the same way as software, hardware can be developed modularly. That is that different hardware blocks can be used to perform a discrete task and these blocks can be interchanged within the overall design to alter the operation of the system. Partial reconfiguration of an FPGA allows the alteration of certain portions of the hardware configuration of the FPGA, while allowing other sections to remain untouched. This is achieved in two distinct ways; static and dynamic partial reconfiguration. Static partial reconfiguration requires the FPGA device to be put in to a non-active or reset mode while the partial reconfiguration takes place, while dynamic partial reconfiguration allows the reconfiguration of certain hardware blocks

of the FPGA while the other hardware elements of the FPGA continue to operate as normal.

2.5.4 A Review of Programmable Logic Applications

Prototyping & Final System Implementation

Prototyping is a common usage for PLDs as they allow flexibility during the system design stage. Smaller PLDs may be used to allow system designers to change a systems logic more easily during product development and testing, while large devices may be included to allow prototyping of a system on a chip (SoC) design that will eventually find its way to production in the form of an ASIC.

The use of a PLD during prototyping allows hardware flexibility, which greatly reduces development time. When the product is ready for large scale production, the PLD can be replaced with a less expensive, though functionally equivalent, hardware alternative.

More recently, with the increased capabilities and reduced cost of modern PLDs, the PLD is often used in the final system implementation, avoiding the added development costs of ASIC development. This is especially true of specialised product designs, where lower production numbers do not allow the product to take advantage of the economies of scale associated with ASIC implementation.

Embedded Processing

More and more PLD vendors are selling or providing processor and peripheral cores and other optimised hardware configuration in the form of Intellectual Property (IP) blocks. These devices are supplied to the PLD system developer as a pre-synthesised and tested block that can be easily integrated in a HDL logic design within the vendors EDA toolset. This allows the streamlining of the system design process and is often used by vendors to demonstrate their devices potential for growth in the SoC area. Many vendors also have more advanced IP blocks which require additional (costly) EDA software to implement.

Re-Configurable Computing

As mentioned earlier, an SRAM-based programmable device can have its internal design altered on-the-fly. This practice is known as re-configurable computing. Though originally proposed in the late 1960's [43], this is still a relatively new field of study. This decades-long delay has been mostly due to a lack of suitable re-configurable hardware. On-the-fly re-programmable logic chips have only recently reached gate densities making them suitable for anything more than academic research. Recently re-configurable computing has found applications in high-end communications, military, and intelligence applications.

Digital Signal Processing on FPGA

In recent years, the development of more advanced FPGA technologies has led to their use in the field of DSP, often in place of a dedicated DSP or DSP ASIC. Grout states that while PLDs were originally used to prototype ASIC designs at lower speeds, with the advancements in high-speed FPGA operation, modern PLDs are becoming the device of choice for use in final DSP applications [44].

“...with the high speed and ability to perform complex digital signal processing operations within a single PLD, the PLD itself is becoming in many cases the choice for design prototyping and for use in the final application” [44]

The FPGAs advantage in the field of DSP lies in their ability to perform multiple tasks in parallel, without the need for expensive multicore technology, through the use of their hardware functionality. Certain MAC architectures have been developed to allow the efficient exploitation of the FPGA in the implementation of high-speed DSP algorithms, such as the distributed arithmetic techniques of computation. [45]

In addition to this, many current FPGA devices have been optimised for the computationally intense operations associated with DSP algorithm implementation. Such FPGAs contain dedicated DSP slices, each containing a high-speed MAC which allows efficient execution of common DSP operations such as filter implementation and series style signal transforms. With this optimisation, coupled with the large amount of parallelism inherent in PLD architecture, higher-end FPGA devices have

reached into the Tera-MAC range, with the Xilinx[®] Virtex 7 series FPGA able to perform over 5 Tera-MACs per second. [46]

In the recent past, many papers have appeared which state that the re-configurable hardware approach to DSP is far superior to the traditional processor based approach [47, 48]. Many comparisons have also been made between the execution of DSP algorithms on purpose specific DSPs and the implementation of the same algorithm on FPGA [49]. FPGA manufacturers have also published white papers claiming the superiority of FPGA implementations of DSP functions over implementation on DSP [50, 51, 52], with Altera[®] claiming a 95% cost reduction through the use of an FPGA in the place of a DSP [53]

Woods *et al* states that while strides have been made with DSPs now providing concurrency in the form of parallel hardware and pipelining of software operations, true parallelisation can only be achieved by a hardware implementation such as that provided by an FPGA [54].

2.6 Conclusion

This chapter has provided an overview of RFID technologies. A brief description of the origins of RFID technology along with an outline of the technological progressions has been presented. A description of the technical operation of RFID systems has been given which describes the operation of various RFID system types, along with the limitations of each particular variety. This has been followed by a brief overview of some of the current applications of RFID systems and a short note on the addition of sensors to RFID tag functionality has been presented.

An alternative to the microprocessor/controller, the PLD, has been described in detail. The types of PLDs and their operation have been presented along with a description of the current state-of-the-art. PLD system development and configuration techniques have been described as well as the applications for which PLDs are currently used. The later part of this section focused on the efficient implementation of DSP algorithms and a strong case for the implementation of DSP algorithms on

FPGA has been made. Finally, the operation and components of a typical embedded system are presented.

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Chapter 3

Animal Auto-ID: Its Place and Standardisation within the Livestock Industry

3.1 Introduction

The current requirement for increased global traceability of livestock and animal-based food products has driven the introduction of mandatory trace-back systems in the European Union (EU) and countries such as Australia, Canada and Japan. This has led to the use of Radio Frequency Identification (RFID) tag based animal Automatic Identification (Auto-ID) systems in many livestock farms, slaughter houses, marts and veterinary facilities and has become mandatory in some jurisdictions. Such Auto-ID systems are often not only used on a national and global scale for food product traceability but also at an on-farm scale as an integral part of an automated precision agriculture management system. [1]



Figure 3.1: Dairy Animal Auto-ID

Initially, the role of animal Auto-ID systems in the dairy sector focused on herd management and labour saving automation, but the focus has now begun to shift to animal Auto-ID for the purpose of animal traceability, food safety and epidemic control. This has become a priority in the livestock sector following several major

food scares, most notably the Bovine Spongiform Encephalopathy (BSE) crisis during the 1990's [2]. This climate has driven the need for a world-wide protocol for livestock identification and traceability. Such protocols are widely used on a national level but, in 1996, the International Standardisation Organisation (ISO) standardised the use of Auto-ID technology for international animal identification in its standards 11785:1996 and 11784:1996 [3, 4]. Further standardisation was introduced for 'advanced' animal transponders in 2003 in ISO standard 14223:2003 [5]. This standard is intended as an addition to the two earlier standards. Together these three standards govern the operation and functionality of RFID-based animal Auto-ID systems. ISO 11785:1996 stipulates the structure of the unique animal identifier number which is to be stored on each animal Auto-ID tag. ISO 11784:1996 governs the technical operation of both the animal Auto-ID tags and readers, including the interaction between adjacent readers.

This chapter will present an introduction to the field of animal Auto-ID, focusing on the Auto-ID of cattle, primarily within the dairy industry. It will begin by outlining the need for livestock traceability and continue with an outline of the roll played by animal Auto-ID in the traceability process. It will then continue with a description of the roll of animal Auto-ID systems in the automation and management of a dairy farm and a description of the integration of an animal Auto-ID system into an automated milking parlour and herd management system. The chapter will conclude with a detailed description of the ISO standards; ISO 11784:1996 and ISO 11785:1996. ISO 14223:2003 will be briefly described as an extension to the core functionality of animal Auto-ID systems.

3.2 Livestock Traceability

Over the past number of decades, the globalisation of the livestock and livestock-based food trade has greatly expanded due to improved technology, processing techniques and the centralisation of food processing facilities. With this globalisation has come an increase in the length of animal-based food supply-chains. This has led to a greater concern for food safety and epidemic control from both government

organisations and the public. With increased concern has come the requirement for the efficient and accurate traceability of livestock over a worldwide network.

Livestock Traceability is defined as the ability to follow a food-producing animal intended to be, or expected to be, incorporated into a food or feed, through all stages of production, processing and distribution. It should be noted that the term 'trace-back' differs slightly in that it is the ability to follow a product back through the supply-chain, but not as it progresses forward through the supply-chain to the finished food-product.

Many nations have made, or are in the process of making, livestock traceability mandatory. As early as 2001, Canada had implemented an individual cattle ID program based on permanent RFID animal tags. This has become mandatory as of July 2005 [6].

Within the EU the traceability of food stuff is governed by directive 178/2002 [7] which came into force on January 1st 2005. This directive has enacted stringent guidelines with regard to the traceability of food product which are offered for sale within the EU. Article 18 of this directive states:

“The traceability of food, feed, food-producing animals, and any other substance intended to be, or expected to be, incorporated into a food or feed shall be established at all stages of production, processing and distribution.” [7]

After the BSE scare of 2001, Japan mandated the traceability of domestic cattle through the supply chain on December 1st 2003 [8]. The US is currently considering a full individual animal ID proposal with the goal of "48-hour trace-back" under the National Animal Identification System [9]. New Zealand is in the process of implementing an electronic identification system for their livestock industries [10], while draft legislation is in place in Europe which advises the voluntary implementation of RFID-based animal identification with the possibility of obligatory introduction on a national basis [11].

3.3 The Roll of Animal Auto-ID Systems in Global Traceability Systems

A global animal traceability system requires the integration of several key components; a system for providing each animal with a unique ID, a method for interrogating this ID in an efficient and reliable manner and a suitable global database in which to store the movements and processes undergone by each animal.

The issuing of a unique identifier number to each livestock animal has been implemented in many countries on a national level. While the structure of an international unique animal identifier number has been standardised by the ISO [4], global implementation is still in its early stages. A database capable of storing animal ID history globally is also a long way off. In his paper, “*Positive, Accurate Animal Identification*”, Dzuik describes the importance of a reliable method for the identification of individual animals in a global animal traceability system. [12]

RFID-based animal Auto-ID systems offer an extremely accurate method for the efficient identification of individual animals based on each animal’s unique identifier number. When compared to manually logged visual ID tags, Auto-ID systems perform to a much higher standard as each Auto-ID tag ‘read’ is electronically ‘double-checked’ using an error detection technique called Cyclic Redundancy Check (CRC). In this way identification errors are kept to an absolute minimum. The CRC process is described in greater detail in section 3.7.4.

Stewart *et al.* in their study of Auto-ID tag read-rates [13], found that HDX animal Auto-ID tags had a successful read rate of 99.9 (± 0.1)%. Those tags which were unsuccessfully interrogated did not produce an incorrect animal ID code but were simply undetected by the tag reader due to tag failure.

To counteract the effects of dishonesty in the industry, once initially programmed the ID-Code present on tags compliant with ISO standard 11785 cannot be altered and tags are not easily replicated.

Although the information contained on RFID-based tags can generally be read by anyone using the standardised reader equipment, work is underway to ensure that RFID technology becomes more secure in future implementations of Auto-ID technology. [14]

While ISO standardisation specifies the use of LF Auto-ID system for animal traceability, organisations such as GS1 are currently promoting the adoption of Ultra-High Frequency (UHF) Auto-ID systems for animal identification. Such a system would bring animal traceability into line with modern supply-chain management systems which largely utilise UHF technology, incorporating the EPCGlobal standardisation [15]. This would allow increased integration of animal traceability systems and supply-chain managements systems, allowing greater traceability of animal-based food products. It is also suggested that UHF systems will improve animal identification through improved tag read-rates and ranges. [16]

3.4 The Roll of Animal Auto-ID Systems in Farm Management and Automation

Auto-ID technology is a vital component of any livestock farm automation system. It has removed the need for manual animal identification during operations such as animal health monitoring, drafting, feeding and cattle milking procedures. This has allowed many of these processes to become entirely automated, allowing for greater herd management processes, more efficient farm operation and extensive labour saving.

Precision agriculture is a farm management practice which uses data taken from many sources throughout the farm to make decisions which will maximise yields while minimising production costs. In livestock farming, the ability to monitor the health, feeding and resulting yield (both quantity and quality) from each animal is vital. Animal Auto-ID allows such monitoring to be performed automatically and efficiently, with the correct positioning of Auto-ID readers in conjunction with other automated devices. Such a system allows individual animal data to be logged

automatically and accurately into a PC-based herd management system and subsequently processed for yield optimisation.

3.5 Animal Auto-ID System Implementation

The standard installation of an Animal Auto-ID system consists of an Auto-ID reader (including a suitable antenna), a PC operating herd management software and a unique Auto-ID tag for each animal to be tracked by the system. Depending on the complexity of the system, a number of Auto-ID readers may be implemented throughout the farm. Figure 3.2 demonstrates the chain through which the animals ID passes, from the Auto-ID tag to the herd management software.

This section will focus on the implementation of animal Auto-ID systems in the dairy parlour environment. Each component of such a system will be presented along with the description of the component's roll in the automation of the parlour and management of the farm.

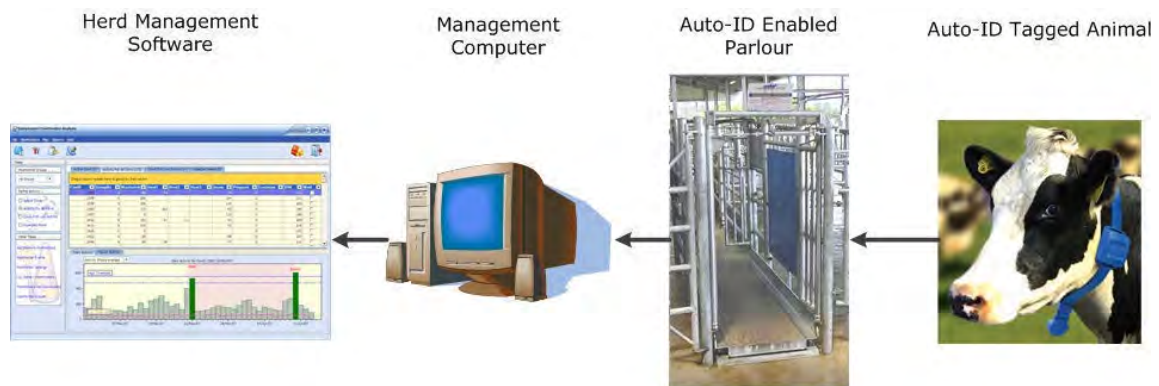


Figure 3.2: Animal Auto-ID Interrogation Path

In addition to the basic components required to read an Auto-ID tag and log the tag information on a computer database, an Auto-ID system can be integrated into a number of other devices to automate the processes of drafting, feeding, health monitoring and yield monitoring.

3.5.1 Livestock Auto-ID Transponders

Animal Auto-ID transponders come in many different formats, with the ear tag variety commonly used in the dairy parlour automation sector. Other formats include the bolus tag which generally resides in the stomach of ruminant animals and injectable tags which are often inserted between the shoulder-blades of animals. As specified by the ISO standard [4] each of these Auto-ID tags is passive in nature. Some national animal traceability schemes specify “*The minimum time that a tag shall be expected to remain functional (electronically) is for the expected life of the animal*” [17]. As the working lifespan of a dairy animal is often in the range of 8 to 10 years, an active tag would not have a suitable lifespan without a prohibitively large battery. See figure 3.3 for examples of these tag formats.

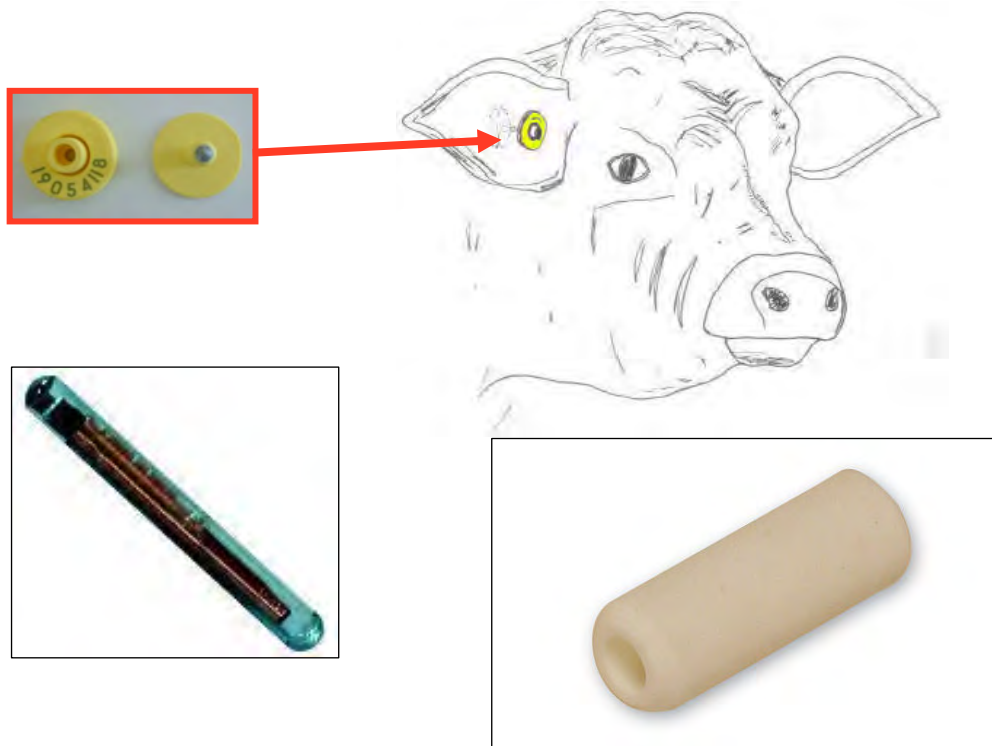


Figure 3.3: Animal Auto-ID Transponders
(Clockwise from top: Ear tag, Bolus Tag and Injectable Tag)

For parlour automation purposes, RFID Auto-ID ear-tags have been found to operate with the greatest range. As they are applied to the animals externally, the activation and tag response signals do not experience the absorption loss encountered as the signal passes through animal flesh. However, this does not mean that all livestock should be tags using ear tags. Ryan [18] found that the type of tag to be used

is highly dependent on the particular type of livestock to be tracked by the system. A clear example is the instance of pigs commonly chewing the ear-tags of other pigs, causing the tag to be destroyed. The IDEA Project found that, while low at 2.32% after 14 months, animal ear tags had the highest failure rates, compared to 0.28% for Bolus tags and 1% for injectable tags. [19]

3.5.2 Animal Auto-ID Transceivers

Animal Auto-ID transceivers, often referred to as readers, perform the task of interrogating animal Auto-ID tags and are a vital component of the Auto-ID system. The operation of these readers is governed by ISO standardisation which is covered in detail in section 3.7.

Many ISO compliant animal Auto-ID readers are currently on the market from major manufacturers such as Texas Instruments[®], Allflex[®] and Goa-RFID[®]. The Texas Instruments[®] Series 2000 TIRIS reader devices [20] are often considered the industry standard in HDX technology, due to the widespread proliferation of TIRIS animal Auto-ID tags and the use of TIRIS systems within the standardisation process.

Due to the industrial nature of this application of RFID technology and the industry led development of ISO standardisation in the area, very little published literature detailing the technical aspects of animal Auto-ID system operation is available. Much of the available literature takes the form of advertising literature created by manufacturers. Recently a number of animal Auto-ID readers have addressed the issue of EMI through the implementation of DSP techniques [21, 22, 23], but no technical papers detailing the operation and function of these readers have entered the public domain.

3.5.3 Automatic Animal Drafting

An Auto-ID enabled drafting gate allows an individual animal to be drafted to a predetermined location based on the ID information received by the Auto-ID system. This allows automated segregation of animals requiring special dietary supplements, health checks or insemination. The operation of such a unit is demonstrated in figure 3.4, where an animal enters the drafting crate, its Auto-ID tag is interrogated and

based upon animal ID number received, the gate swings into the correct position to draft the animal to the desired location.

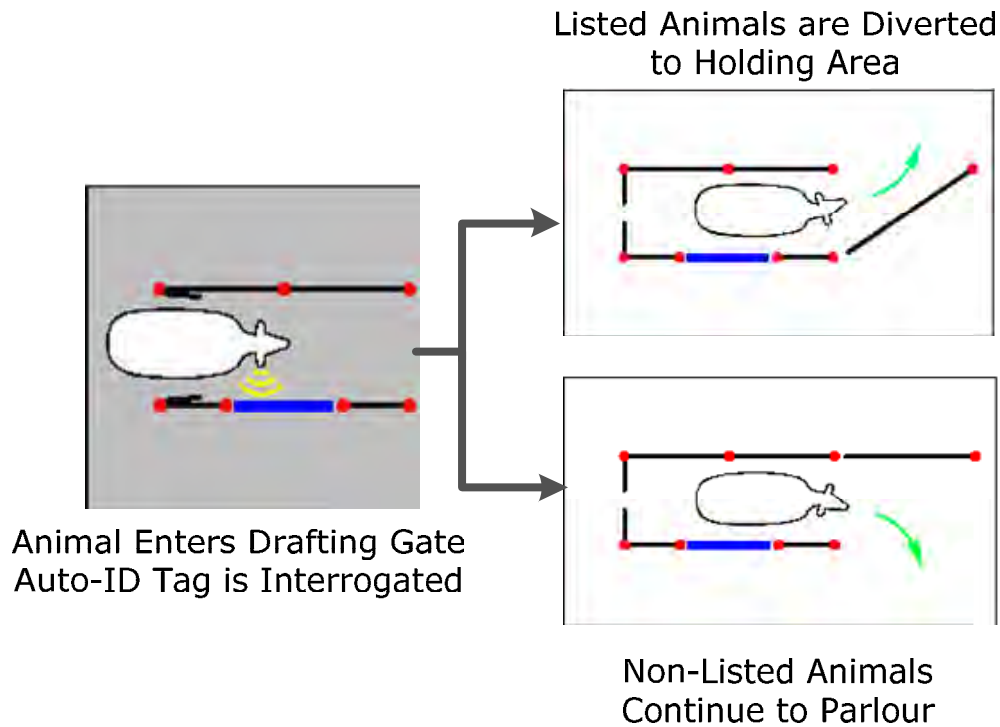


Figure 3.4: Auto-ID Enabled Drafting Gate Procedure

3.5.4 Automatic Animal Yield and Health Monitoring

Within a dairy farm, an Auto-ID system can be used as an integral part of animal health screening and yield monitoring. Once the milking stall location of each animal is determined by the Auto-ID system, yield monitoring data can be easily associated with an individual animal. Through the use of Auto-ID enabled weighing platforms, fluctuations in animal weight can be automatically monitored. With the addition of biometric sensors to the milking lines, the properties of the milk can be monitored for irregularities and again automatically associated with each animal ID, drawing the user's attention to potential animal health issues such as mastitis and ketosis.

Advances in sensor technologies have allowed tags to incorporate sensors into their make-up. This leads to the potential for Auto-ID tags to include temperature, moisture and light sensors which may provide useful additional animal monitoring. [24]

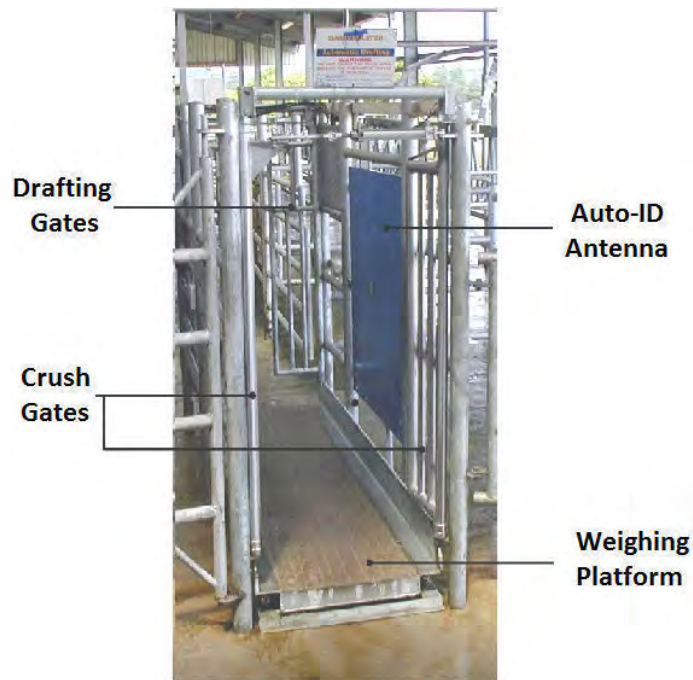


Figure 3.5: Cattle Drafting Crate with Integrated Auto-ID Antenna

3.5.5 Issues Affecting the Operation of Current Animal Auto-ID Systems

Electromagnetic Interference

Within an agricultural environment, Auto-ID systems can suffer greatly from Electromagnetic Interference (EMI) from other devices operating in the vicinity of the readers. As animal Auto-ID systems operate within an ISM frequency band below 135 kHz, devices such as wireless headphones, other RFID systems, unshielded power invertors, light fittings and sonic pest control devices can operate on similar frequencies without limitation. Off-farm sources of EMI, such as Low Frequency (LF) transmitters, have similar effects on animal Auto-ID systems. Each of these factors can lead to cross-interference between the animal Auto-ID system and other devices, resulting in a reduced read-range and 'missed-reads'. The EMI present in an agricultural environment is described in detail in chapter 7.

Dual Standardisation

The ISO standards for RFID-based animal Auto-ID specify the use of two differing RF interface protocols, that of Full-Duplex (FDX) and Half-Duplex (HDX) [3, 4]. These standards are described in detail in sections 3.6 and 3.7. The use of two

different types of tags requires installation of a dual reader system in an agricultural facility, in order to ensure the identification of all animals. This is especially true in such locations as marts, slaughter houses and veterinary facilities where the user has little control over the type of tags applied to each animal. To counteract this, the ISO standards specify that compliant readers must have the ability to interrogate both tag types. In practise many Auto-ID readers can only interrogate a single tag type [25, 26].

Many animal Auto-ID systems operate using the air interface specified by the ISO standards, but do not employ the animal tag ID-code structure specified by the ISO. Such tags set the ‘animal flag bit’ of the code to ‘0’. These tags are often referred to as ‘industrial coded’ tags and are not officially intended for use with animals. [27]

3.5.6 Effects of ‘Missed Reads’ on Farm Automation Systems

As described earlier, an animal Auto-ID system is a vital component of advanced automated milking parlour. If the parlours Auto-ID system cannot successfully read animal Auto-ID tags with a high rate of reliability, severe knock-on effects can result within the automated parlour.

During visits to dairy parlour facilities with high levels of on-site EMI with the Dairymaster[®] service team, in both Ireland and Germany, the effects of animal Auto-ID system ‘missed-reads’ were witnessed. A ‘missed read’ of an animal tag on entry to the parlour has the direct result of not only having an unidentified animal present in the parlour, but also an extra animal present with regard to those believed to be present by the system. This is a serious issue given the limited number of milking stalls available.

At this point the parlour operator must intervene to correct the system by manually entering the missed animal’s ID number, a task often made difficult by the environment and the difficulty in gaining sufficient access to the animal to allow the visual reading of the ear tag number. Given that the goal of any automated milking parlour is to minimise the need for operator intervention, this situation is one that must be avoided.

With respect to automated animal drafting for veterinary purposes, a missed-read can lead to a problem animal (an animal requiring veterinary treatment) remaining with the main body of the herd when it is required to be separated. For smaller farms it is an inconvenience to manually monitor the animals entering the parlour, and isolate ‘missed’ animals for visual inspection. For larger farms, with upwards of 1000 animals, it can be almost impossible to identify and locate the ‘missed’ animal within the herd through visual inspection of animal tags and manual separation. The result is that animals which require veterinary attention will remain with the main herd when they should be drafted to a holding area for treatment, resulting in a degrading of the overall herd health. Also, milk from animals which is unsuitable for human consumption may remain un-diverted, with the result of contaminated milk entering the food-chain.

3.6 ISO 11784:1996

Radio-Frequency Identification of Animals – Code Structure

ISO standard 11784:1996 defines the structure of the 64-bit identification code which is to be stored on an animal Auto-ID transponder [3]. This standard specifies the inclusion of information relating to the animal which has been tagged, such as the unique national animal identifier code, the country in which the tag was issued, the number of times the animal has been retagged, along with extra fields reserved for user information and future use. Compliance with this standard allows the global interpretation of animal Auto-ID data leading to a greater potential for comprehensive global animal traceability. The structure of the bit-stream to be stored on each animal Auto-ID tag is presented in table 3.1.

Bit Number	Purpose	Description
1	Animal Flag	Set to '1' if the tag is an animal tag
2 – 4	Retag Counter	Initially '000'. The binary number is incremented if the animal is retagged with an identical ID number
5 – 9	User Information Field	Miscellaneous information as designated by the country
10 – 15	Reserved	Set to '0'
16	Data-block Flag	Set to '1' if additional information is contained in the ID trailer. Otherwise set to '0'
17 – 26	Country Code	Identifies country where the tag was issued
27 - 64	National ID Code	Animal ID code, unique within each country

Table 3.1: Animal Identifier Code Structure

3.7 ISO 11785:1996

Radio-Frequency Identification of Animals – Technical Concept

The ISO 11785:1996 standard specifies the use of LF passive transponders for the automatic identification of animals [4]. The standard details how an animal Auto-ID transponder should be activated by an Auto-ID interrogator and the manner in which the ID information stored on the tag should be transmitted and subsequently received and deciphered by the transceiver. This standard also specifies that a single transceiver system should be capable of reading both Full-Duplex (FDX) and Half-Duplex (HDX) Auto-ID transponders. Also outlined is the method for which adjacent transceivers should synchronise with respect to the activation and read cycles.

This section will outline the specified operation of the components of an animal Auto-ID system, beginning with the Auto-ID transponders (both FDX and HDX), followed by the tag interrogation system.

3.7.1 Full Duplex Based Animal Auto-ID System

A passive FDX Auto-ID tag transmits its stored data back to the transceiver while the activation signal is still present through a system of antenna circuit load

modulation. It does not have the ability to store the power gained from the activation field and therefore the transponder must have the ability to both receive power from the EM activation field and transmit data simultaneously. ISO 11785:1996 specifies that the activation signal for this tag should be of frequency 134.2(\pm 13.42) kHz and of suitable amplitude to provide power to the tag circuitry. [4]

An FDX tag will remain dormant until it is provided with a suitable activation signal, upon which it will activate and begin transmitting the identification data stored on the tag back to the reader device. The data-stream of an FDX tag must be transmitted using an Amplitude Shift Key (ASK) modulation scheme with Modified Differential Bi-phase encoding. The frequency of the amplitude modulated signal emitted by the FDX tag must be in the range 129-133.2 kHz or 135.2-139.4 kHz. 32 cycles of the activation field are allocated for transmission of each bit. 8-cycles are allowed for a low-to-high amplitude transition. This results in a transmission bit rate of 4195 bit/s.

The response from a FDX tag can be identified by an initial 11-bit Header of the form "00000000001". Apart from this header, all of the bit-stream is transmitted in 8-bit blocks, with each block being trailed by a binary '1'. This eliminates the chance of the header sequence being repeated within the data-stream. The header is followed by a 64-bit (8 x 8-bit blocks) animal ID-Code which is in turn followed by a 16-bit (2 x 8-bit blocks) CRC error detection segment. A final 24-bit (3 x 8-bit block) trailer is used to store any additional information required. The structure of the 64-bit animal ID-code can be seen in table 3.1.

3.7.2 Half Duplex Based Animal Auto-ID System

A passive HDX tag has the ability to store the energy it receives from the activation signal. This energy is then used to transmit the stored data once the activation field has dropped to a level of -3 dB. ISO 11785:1996 specifies that the activation signal for this tag should be of frequency 134.2(\pm 13.42) kHz and of suitable amplitude and duration to charge the reservoir capacitor of the tag. A HDX tag must remain dormant until its reservoir capacitor has been sufficiently charged by a suitable activation signal. It then enters a wait mode until the activation field drops. [4]

It will begin to transmit its data between 1 and 2 ms after the strength of the activation field drops by -3 dB. If the transceiver does not receive a HDX tag header which indicates the beginning of a transmission from a HDX tag before 3 ms have elapsed, the transceiver will reactivate the activation field. If a response from a HDX tag is received within 3 ms the tag must complete its transmission within the next 17 ms, before the activation field will be reactivated.

HDX tags use a Frequency Shift Key (FSK) modulation scheme with non-return to zero encoding to transmit its stored data. The transmission of a 124.2 ± 2 kHz signal for a 16 cycles represents a binary '1' and the transmission of a 134.2 ± 1.5 kHz signal for 16 cycles represents a binary '0'. This results in a transmission bit rate of 7762.5 bit/s for binary '1's and 8387.5 bit/s for binary '0's.

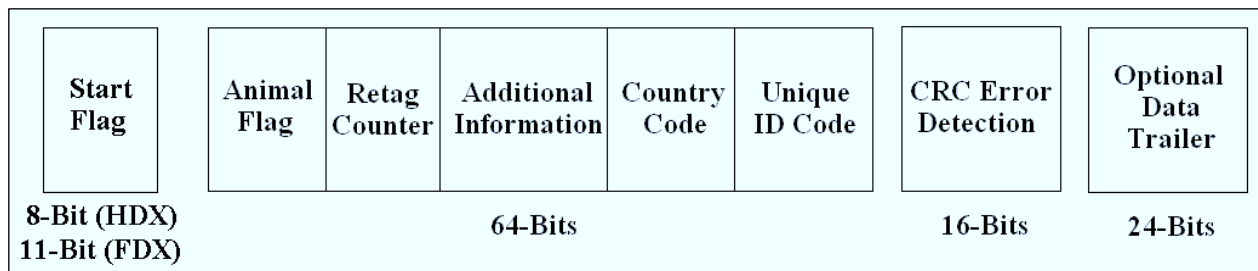


Figure 3.6: Animal Auto-ID Code Structure

The structure of the bit-stream transmitted by an animal Auto-ID tag is as follows. The beginning of a HDX tag transmission is identified by an 8-bit header of the form "01111110" followed by the 64-bit unique animal ID-Code. A 16-bit CRC error detection number is then transmitted and finally a 24-bit trailer is appended if additional information is required.

3.7.3 Auto-ID Transceiver

A transceiver designed for the interrogation of animal Auto-ID tags, as specified in ISO 11785:1996, has two specific tasks: the creation of an activation field capable of activating both FDX and HDX tags within a suitable range and the reception and demodulation of both FDX and HDX tag responses.

The reader must perform the activation of both FDX and HDX tags. This is accomplished through the use of an electromagnetic (EM) activation field of frequency $134.2(\pm 13.42)$ kHz and of suitable strength to energize the tags appropriately. To facilitate the activation and reception of the resulting data-stream from an FDX tag, an activation period of 50 ms is specified by ISO 11785:1996. This activation period may be extended to 100 ms if an FDX signal is received but not validated within this period. [4]

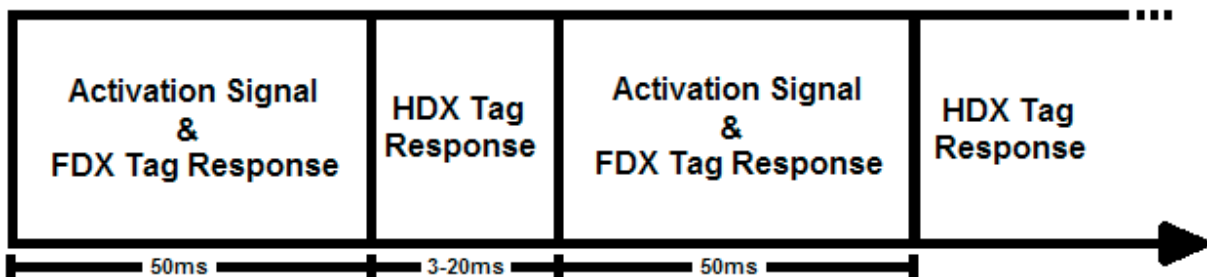


Figure 3.7: Timing Diagram for Reading an Auto-ID Tag

This activation period of 50 ms also facilitates the charging of any HDX tags which may be within the activation field. Upon completion of the activation period, the 134.2 kHz activation signal is then ceased for 3 ms to allow any HDX tags within range to respond. This 3ms period begins immediately from the instant the activation signal on the antenna drops to a level of -3 dB and is referred to as the “listening period”. It is also specified that the activation field must drop from -3 dB to -80 dB within a period of 1 ms after the commencement of the listening period.

If, during this 3 ms listening period, a data-stream from an HDX tag is received, the listening period is extended to a total of 20 ms. If a data-stream from a HDX tag is not received during the 3 ms listening period the activation signal is resumed. For the purpose of synchronisation of multi-reader systems, every tenth cycle will have a fixed cycle of 50 ms activation period followed by a 20 ms pause. A mobile transceiver must also have the ability to detect the activation of any other transceiver within its vicinity. If another activation field is detected, the mobile transceiver must synchronise its activation/listening cycle with that of the detected reader.

The second function of the reader system, the reception and demodulation of the response from both FDX and HDX auto-ID tags, requires two separate operations. The response from an FDX tag occurs during the activation period. This requires that the reader has the ability both transmit the activation signal and receive and demodulate the tags response simultaneously. An FDX tag's response takes the form of an ASK signal within the frequency range 129-133.2 kHz or 135.2-139.4 kHz. The reader must have the ability to demodulate this ASK modulation scheme with Modified Differential Bi-phase encoding [4].

The response from the HDX signal occurs within the listening period. This signal takes the form of a FSK modulated signal varying from 122.2 kHz to 135.7 kHz and the reader must be capable of demodulating this signal.

3.7.4 CRC Error Detection Routine

Cyclic Redundancy Check (CRC) error detection techniques were originally developed for use in hard-drives but have now found widespread application in the field of data transmission. Even though the CRC error detection routines cannot correct an error, it is a highly reliable method for the detection of errors occurring during the transmission of raw data. The CRC operates as a checksum on the data to be accurately transmitted. The CRC value is calculated before transmission and then appended to the data to be transmitted. Once the data block with the appended CRC is received following transmission, the CRC operation is repeated, allowing any error which may have occurred during transmission to be detected.

The CRC value is generated by dividing the data stream (left-shifted by the length of the CRC polynomial) to be transmitted by the CRC polynomial. The remainder of this operation is taken as the CRC value and appended to the data block. The error checking routine can be performed by dividing the data block with the appended CRC value by the CRC polynomial with the expected result of zero remainder. If the remainder of this operation is anything other than zero, an error has occurred during transmission.

ISO 11784 specifies the use of a 16-bit CCITT CRC error detection system, using the 0x1021 polynomial. At the time of tag memory programming, the CRC-16 is

calculated for the 64-bit unique animal ID-code and appended to the code to create an 80-bit data stream, which is then stored on the tag. Once a tag has been successfully interrogated by an Auto-ID transceiver, the CRC operation can be carried on the received 80-bit data stream, with a non-zero result indicating a transmission error. This provides a reliable verification of the ID-code bit-stream.

3.8 ISO 14223:2003

Radio Frequency Identification of Animals – Advanced Transponders

ISO 14223:2003 outlines the operation of ‘advanced’ transponders and is described as an extension to ISO 11784:1996 and 11785:1996. Under ISO standardisation, an advanced animal Auto-ID transponder has the same functionality of a standard animal Auto-ID transponder with the added facilities of “the storage and retrieval of additional information (integrated database), the implementation of authentication methods and reading of the data of integrated sensors” [5].

This standard is divided into 3 sections; ‘Air Interface’ which describes how the transceiver and transponder should communicate, ‘Code and Command Structure’ which outlines the information request which can be made by the transceiver to the transponder and ‘Applications’ which described the uses of such an advanced transponder system. For the operation of Advanced Animal Auto-ID tags in accordance with this standard, the system must also conform to ISO 11784:1996 and ISO 11785:1996, described earlier in this chapter. Section 3.6 describes the structure of the binary identifier number to be stored on an animal Auto-ID tag. Bit 15 of this binary number is reserved by ISO 14223-1 for the flagging of a tag as an ‘Advanced’ tag. Bit 16 is reserved to flag the presence of additional information on the ‘Advanced’ tag.

After a tag (HDX or FDX) has been successfully interrogated in ISO 11784 mode and the reader has determined that an ‘Advanced’ tag is in the interrogation zone, the reader may choose to switch the tag into ‘Advanced’ mode. This is done by transmitting a ‘Start of Frame’ signal within the switch window. Once in advanced

mode, advanced request commands can be transmitted to the ‘Advanced’ tag by the reader and the advanced tag will respond accordingly. Two different procedures are implemented for querying advanced tags depending on whether the advanced tag is of the HDX or FDX variety

3.8.1 FDX-ADV Querying Procedure

For FDX Advanced (FDX-ADV) tags to be placed in advanced mode, the activation field must be firstly turned off for at least 5 ms and then reactivated to transmit the SOF command to the tag. Communication from the reader to the FDX-ADV tag is achieved through ASK modulation using Pulse Interval Encoding.

Once the FDX-ADV tag has entered advanced mode, read/write or inventory operations can take place, depending on the commands sent by the reader module. Once all advanced operations have been completed, the reader ceases the activation field for at least 5 ms to reset the tag.

3.8.2 HDX-ADV Querying Procedure

For HDX Advanced (HDX-ADV) tags to be placed in advanced mode they must be recharged after the initial ISO11785 operation. To facilitate this, the activation field is reinstated for a period of between 5 ms and 20 ms. The exact duration is dependent on the request to be sent to the tag as the tag requires different amounts of energy to process different requests. Upon completion of the charge period, the reader can transmit a request to the tag using a Pulse Interval Encoded ASK modulation scheme. The reader then switches off the activation field to allow the HDX-ADV tag to respond with the requested information. The HDX-ADV transponder responds using a FSK modulation scheme. Multiple recharge/tag query cycles are permitted.

3.9 Conclusion

This chapter has outlined the rationale behind the implementation of Auto-ID systems within the livestock industry and the need for the comprehensive traceability of livestock and animal derived food products. An overview of the implementation of electronic animal Auto-ID in the livestock industry, focusing on parlour automation

within the dairy industry has also been presented. Of particular note to this thesis are the causes of ‘missed reads’ and their effect on parlour automation, detailed in sections 3.5.5 and 3.5.6 respectively. Such affects justify the focus of this thesis.

This chapter has also presented the ISO standards which govern the use of RFID-based animal Auto-ID for the accurate, efficient identification of livestock. Firstly the structure of the unique animal identifier code is described as standardised in ISO 11785:1996. Then a detailed review of ISO 11784:1996, the standard governing the activation of the ID-tags and the transfer of information from the tags to the interrogator, is presented. Finally the standardisation of the operation of advanced animal Auto-ID tags, ISO 14223:2003, is outlined.

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Chapter 4

Case Study 1: Low-Frequency Antenna Circuit Auto-Tuning & Adjustment

4.1 Introduction

In order for an Animal Auto-ID reader to activate a Half-Duplex (HDX) or Full-Duplex (FDX) passive animal Auto-ID tag, the reader must generate an electromagnetic (EM) activation field which will provide power to the animal Auto-ID tag. Such a power transfer occurs through the means of inductive coupling between the loop antenna of the reader module and the tag, as described in detail in Chapter 2. This is best achieved when the antenna circuits of both the tag and the reader are tuned to resonate at the system's frequency of operation. ISO compliant animal Auto-ID systems have an operating frequency of 134.2 kHz [1]. The low-frequency (LF) magnetic coupling antenna circuits used by both the reader module and tag take the form of a resonant loop antenna circuit, which equates to an inductance, and a capacitance connected in series.

The inductance and capacitance values of the antenna circuit of an animal Auto-ID tag are set at manufacture and are not designed to be altered after fabrication. As the loop portion of the antenna circuit of an animal Auto-ID reader is physically larger than that of a tag, its inductance is susceptible to considerable variations due the composition of materials in its immediate environment. A change in the inductance of the loop will cause the resonant frequency of the antenna circuit to change and therefore reduce the circuit's ability to transmit and receive EM signals to and from an Auto-ID tag at the frequency of 134.2 kHz. Therefore, the antenna circuit of an Auto-ID reader is manufactured to be easily re-tuneable to account for changes in the composition of the antennas environment.

As the ability of the antenna circuit to receive and transmit signals at a frequency of 134.2 kHz is dictated by the antenna circuit tuning, de-tuning of the antenna circuit has long been used in the field as a method for limiting the read-range of inductively

coupled Auto-ID systems. By slightly detuning the antenna circuit of the reader, the magnitude of the activation field is reduced, reducing the range at which an Auto-ID tag can be activated, effectively reducing the read-range of the system. This slight detuning also reduces the magnitude of the tag signal received by the reader, resulting in reduced interrogation reliability in the presence of EMI.

4.2 Dairymaster[®] Animal Auto-ID System Antenna Tuning

The Dairymaster[®] Animal Auto-ID system is built around Texas Instruments[®] Series 2000 RI-RFM-007B RFID module [2], shown in figure 4.1. This module contains a capacitor bank consisting of six capacitors for the purpose of tuning the antenna circuit to resonate at 134.2 kHz. These six capacitors are incorporated into the antenna circuit through a series of six jumpers, which allow the circuit to be tuned to resonate at the specified frequency when an antenna with an inductance value of between 26 and 27.9 μ H is connected to the module.



Figure 4.1: Texas Instruments[®] Series 2000 RI-RFM-007B RFID Module [4]

The operation of tuning the antenna circuit involves the repeated reconfiguration of the capacitor jumpers, followed by measurement of the antenna voltage. The jumper configuration generating the highest antenna voltage is said to be the closest approximation of the capacitance required to achieve resonance at 134.2 kHz. The

current system calls for the manual insertion/removal of these jumpers and measurement of the antenna voltage, using a portable multi-meter / oscilloscope. Within industry, an animal Auto-ID reader is not considered a user serviceable device. Therefore, on each occasion when a system needs to be retuned to give an optimum read-range, a technician is required to visit the installation and perform the operation.

Texas Instruments[®] have in the past marketed a device for the automated tuning of their Series 2000 Auto-ID module. This item is no longer on the market, but can be purchased as part of a complete Auto-ID solution, the Texas Instruments[®] SERIES 2000 READER S251B. This item is priced at US\$600.00 in quantities of 1000, directly from Texas Instruments[®] [3].

4.3 Case Study Objectives

The main objective of this case study was the development of a device to automatically configure the capacitor bank of the antenna circuit of the Texas Instruments[®] Series 2000 RI-RFM-007B RFID Module. This configuration allows the reader antenna circuit to operate in resonance and hence allow the antenna to create an EM-field with maximum efficiency. This in turn allows the optimum transmission of the EM signal between the reader and the Auto-ID tag and visa-versa, resulting in the best possible read range of the Auto-ID system.

It must also be noted that it is not desirable in all cases to have the Auto-ID system operating to the maximum of its abilities. Often the maximum range of the system is too great for the purpose it is designed to achieve. A large read range can have adverse effects on the overall performance of the Auto-ID system by causing 'double reads' and reading tags outside of the zone in which they need to be detected. An excessively strong EM activation field may also hinder the operation of other Auto-ID systems operating in the vicinity. Therefore it must also be possible to intelligently reduce the magnitude of the EM activation field, and hence the read range, of the system.

The only facility to alter the read range of the current Dairymaster[®] Auto-ID system is by the configuration of 6 jumpers within the tuning capacitor bank which serves to create an impedance match between the output stage of the Texas Instruments[®] module and the Dairymaster[®] loop antenna. By detuning the antenna circuit, (i.e. initiating a capacitance value slightly different from that required for the system to operate in resonance) the efficiency of the antenna circuit is reduced, thereby reducing the strength of the activation field and the Auto-ID system read-range.

Further research was undertaken in this case study into a more suitable way for read-range adjustment using variation of the system power supply. It is acknowledged that the implementation of such a system may be impossible using the current Texas Instruments[®] module as initial investigation found that the system supply voltage was regulated within the module. Such a system may be integrated into future Animal Auto-ID readers.

4.4 Auto-ID Antenna Circuit Tuning

The antenna circuit of an inductively coupled Auto-ID system can be modelled as a Resistance-Inductance-Capacitance (RLC) circuit. This antenna circuit is driven by a high current amplification stage producing a 134.2 kHz squarewave of amplitude 12 Vp-p. This results in the excitation of the resonant antenna circuit, creating an antenna voltage in the region of 300 Vp-p. It is important to note that this squarewave is only present during the reader's activation cycle and is not present during the readers listening period. For the correct operation of this Auto-tuner device, the reader module must be set to operate in a continuous activation cycle until auto-tuning is complete. This is achieved by applying a 0 V or ground signal to the control pin of the module. [2]

When an RLC circuit is in a state of resonance the complex impedance of the capacitive and inductive elements are equal in magnitude but 180° out of phase. Therefore the inductive impedance (Z_L) and the capacitive impedance (Z_C) exactly cancel in accordance with equation 5.1. The result is that the impedance of the circuit

is entirely due to the Ohmic resistance of the circuit elements. This allows the current flow through the antenna and voltage across the antenna to be at a maximum, as given by equations 5.2, 5.3 and 5.4. At this point the antenna circuit is operating at its most efficient and producing the strongest possible activation field. [5]

$$|Z| = \sqrt{R^2 + j(X_L + X_C)^2} \quad (4.1)$$

where, $X_L = j2\pi fL$ and $X_C = \frac{1}{j2\pi fC}$

Therefore the maximum current flowing in the circuit can be calculated as:

$$I_{MAX} = \frac{V_{CC}}{R_{OHMIC}} \quad (4.2)$$

where Vcc is the voltage applied to the circuit.

The maximum voltage present on the antenna is given by:

$$V_{MAX_ANTENNA} = X_L \times I_{MAX} \quad (4.3)$$

$$f_R = \frac{1}{2\pi\sqrt{LC}} \quad (4.4)$$

Where it is desirable to reduce the strength of the activation field, the antenna circuit must be detuned from its resonant state. By altering the tuning capacitance from the value which achieved resonance for the system, the capacitive and inductive impedances of the system (X_C and X_L) are no longer equal in magnitude and therefore no longer cancel, resulting in an impedance value greater than the systems ohmic impedance, consisting of ohmic, inductive and capacitive impedances in accordance with equation 4.1.

In practice, Auto-ID antennas are entirely enclosed as shown in figure 5.2 and therefore it is unlikely that the air-core of the antenna loop will be replaced by some other medium once the system has been deployed. On the other hand, it is possible that an item, such as a large metal object, could be placed in close vicinity to the antenna in such a manner that it can have a large effect on the inductance of the antenna loop. In practice, this situation is encountered regularly by Dairymaster[®] as their Auto-ID antennas are mounted on large steel drafting gates as can be seen in figure 5.2 or similarly constructed mounting frames.



Figure 4.2: Dairymaster[®] Auto-ID Antenna Mounted on Drafting Gate

According to equation 4.5 the inductance of the antenna loop is directly proportional to permeability of the core material and therefore a steel-core antenna would have an inductance 700 times that of a similar air core antenna. In many applications an air-core loop is used and therefore the permeability is taken as $4\pi \times 10^{-7}$ H/m. Metals (and some other materials) have a much higher permeability than air, for example the permeability of steel is 875×10^{-6} , 700 times larger the permeability of air.

$$L = N^2 \mu R \cdot \ln\left(\frac{2R}{d}\right) \quad (4.5)$$

where μ represents the permeability of the core of the loop, N represents the number of windings, R is the radius of the antenna loop and d is the diameter of wire used. [6]

During testing it was found that the presence of a large steel structure, such as a drafting gate as those produced by Dairymaster[®], used to mount the antenna had the effect of increasing inductance of the loop antenna by as much as 10 – 15%.

4.5 System Requirements

This Auto-tuner is designed to work specifically with the Texas Instruments[®] Series 2000 RI-RFM-007B RFID module [2]. The antenna circuit of this module has a permanent capacitance value which approximates the capacitance required to provide an impedance match to a 26 μ H antenna, the largest inductance value accepted by the module. A series of six capacitors are also provided which can be added to the antenna circuit to provide an impedance match between the antenna circuit and the antenna driver circuit and so allow the system to operate in resonance.

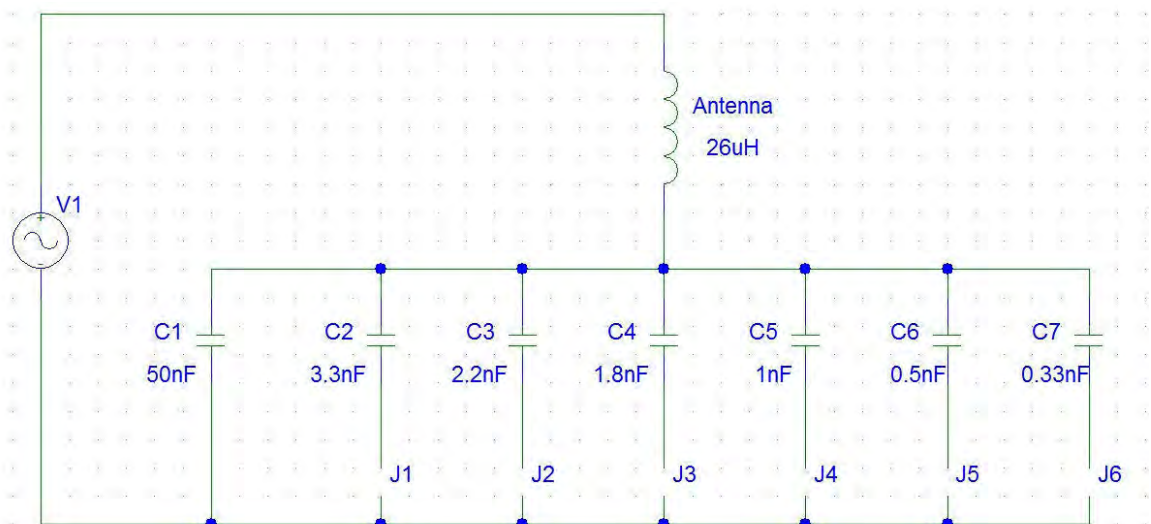


Figure 4.3: Antenna Circuit Schematic

A representative schematic of the antenna circuit is shown in figure 5.3, where the power stage is represented by an AC voltage source. The inclusion of the antenna circuit tuning capacitors is controlled by a set of six jumper pins. When a jumper is inserted across a specific pin, the associated capacitor is incorporated into the antenna circuit.

In all there are 64-possible jumper configurations. The auto-tuner must automatically cycle through each jumper configuration and analyse the antenna voltage resulting from each. Based on these results it will decide on the jumper configuration which most closely approximates the capacitance required to ensure resonance of the antenna circuit for the specific antenna in use by the system.

To accommodate instances where it is undesirable for the system to operate at maximum efficiency a ‘step-down facility’ will be available. This will involve the population of a table, listing all possible jumper configurations in order of descending resulting antenna voltage. The system will then be able to reduce the antenna voltage by stepping through this list. With each successive reconfiguration of the jumpers the antenna voltage will decrease until the desired read-range is achieved.

4.6 System Overview

The auto-tuner device is based around the Atmel[®] ATmega16 Microcontroller [7]. The ATmega16 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. It can operate at clock speeds of up to 16 MHz with throughputs approaching 1 Million instructions per second (MIPS) per MHz. It also contains peripheral devices such as two 8-bit timer/counters, one 16-bit timer/counter, internal and external interrupts and an 8-channel, 10-bit ADC.

This microcontroller controls the alteration of the jumper configuration applied to the Auto-ID module and the processing of the resulting antenna voltage levels. This device has been chosen as it meets the requirements of sufficient processing power, suitable number of I/O ports and in-built Analogue-to-Digital Converter (ADC).

The auto-tuning system will be connected to the module via an IDT 7-by-2 header ribbon cable. Header J3 on the reader module provides connection to the 6 jumper terminals of the switching action of the auto-tuner. Access to the antenna voltage is also provided via header J3 on the ‘antenna circuit test point’ pin.

In the field, the Dairymaster[®] Auto-ID control board controls the operation of the Texas Instruments[®] Auto-ID module, via a control signal squarewave. The high cycle of the waveform activates the modules transmit stage, while the low cycle activates the listening period. The ISO standards specify for HDX animal tag activation, an Auto-ID module should transmit its activation signal for 50 ms and then enter listening mode. For the operation of this auto-tuning system, the module must be set to transmit mode for the entire auto-tuning process. This allows the DC signal generated by rectifying and smoothing the antenna voltage signal to have a smoother profile with less ripple.

4.7 Configuration of Jumpers

The microcontroller is used to generate a 6-bit binary count on one of its ports. This binary count is used to cycle through the 64 possible jumper configurations available on the Texas Instruments[®] module. Initially this binary count controlled the operation of a set of 6 relays which were used to simulate the insertion of a jumper. This allowed a physical connection between the jumper pins.

As relays proved to be prohibitively expensive, they were replaced with low on-resistance, high-voltage MOSFETs. The IRF730 N-channel MOSFET [8] was chosen as it has suitably high-voltage drain-source capabilities (400 V) and a low source-drain on-resistance of approximately 1 Ω . This compares very well with the connection resistance provided by the relays, but at a fraction of the cost. The gates of these MOSFETs are controlled by the microcontroller via a current/voltage buffer to ensure only a minimal current will be drawn directly from the I/O ports of the microprocessor. This buffer also provides greater insulation for the microcontroller in case of malfunction, as extremely high voltages (up to \sim 400 V) may be present on the drain of the MOSFETs.

In addition to these MOSFETs, a single Light Emitting Diode (LED) is also associated with each jumper. This LED illuminates to indicate the activation of a MOSFET and hence indicates the insertion of a specific jumper. Upon completion of the antenna tuning process, the Auto-tuner device can be removed from the system and replaced with the insertion jumpers in the positions indicated by the LED's.

4.8 Antenna Voltage Measurement

The magnitude of the Auto-ID reader antenna voltage is analysed using the built-in Analogue-To-Digital Converter (ADC) on the Atmel[®] Mega16 microcontroller. This ADC has a 10-bit resolution, a maximum sampling frequency of 15 kHz and an input voltage range of 0 to V_{cc} (in this case 5 V).

The signal present on the antenna of the Dairymaster[®] Auto-ID reader system takes the form of a high-voltage sine-wave with a maximum magnitude often in excess of 300 V_{p-p} and a frequency of 134.2 kHz. As the voltage range of this waveform is far in excess of that which can be accurately converted using the in-built ADC, this voltage must be reduced to a representative level. As the frequency of the waveform is also too great to be captured by the ADCs sampling frequency, it will be converted to a DC voltage.

A diode bridge full-wave rectifier, in conjunction with a smoothing capacitor of 1 μ F, is used to convert the 134.2 kHz antenna voltage waveform to a representative DC voltage level. A 1 μ F capacitor was chosen as it provided a suitable trade-off between ripple rejection and voltage level transience time. To reduce the effects of the auto-tuner waveform capture circuitry on the waveform being measured, 1nF capacitors are inserted into the lines connecting the antenna to the full-wave rectifier.

A voltage divider is used to reduce this DC voltage to a level which can be safely presented to the ADC of the Atmel[®] Mega16 microcontroller. As the ADC has an input range of 0 – 5 V, the voltage divider will reduce the rectified antenna voltage in

a ratio of 100:1. The ADC then converts the presented voltage level to a 10-bit binary number which can be easily processed by the algorithm.

4.9 Embedded Software Algorithm

The Atmel[®] Mega16 can be programmed using the Atmel[®] STK500 [9] development board and associated AVR Studio development environment [10]. This development environment incorporates an AVR-GCC plug-in which allows the compilation of C-based microcontroller code into machine code. A flow diagram of the software algorithm is presented in figure 4.4.

Firstly a 64 x 2 cell array is created to hold each jumper configuration and corresponding voltage level information. Upon completion of each jumper configuration initialisation and subsequent voltage measurement, each voltage level (10-bit binary number) and associated 6-bit jumper configuration is entered into the 64 x 2 cell array. Each entry into the array is ordered according to its voltage level, with the highest voltage and associated count value in the first row (1 x 2) of the array and thereafter in order of descending voltage levels.

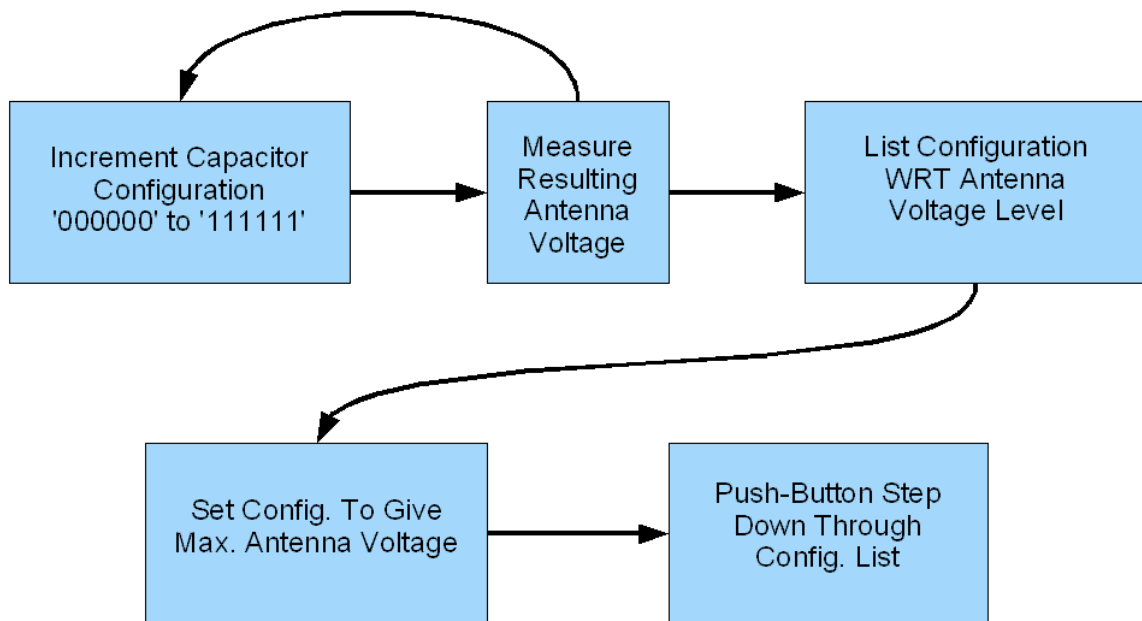


Figure 4.4: Block Diagram of Microcontroller Code Operation

The microprocessor must create a 6-bit binary count on one of its four input/output ports, as shown in the pseudo-code below. The output of this I/O port will be applied (via a buffer) to the gates of the jumper MOSFETs. This count must cycle from '000000' to '111111', which allows the Auto-tuner to cycle through each of the 64 possible jumper configurations, with a '0' representing an open jumper and a '1' representing an inserted jumper. After the initialising of each jumper setting, the microprocessor ADC analyses the DC representative voltage of the signal present on the antenna.

```
Count = 0b00000000;  
While (PORTB < 0b01000000)  
{  
    PORTB = count;  
    Count++;  
}
```

During testing it was found that this antenna voltage level cannot be read instantaneously after the jumper change has been initialised. This is due to transient nature of the capacitive and inductive elements of the system under test. If a change in the antenna circuit capacitance value is made, it takes a period of time for a steady waveform to become present on the antenna circuit, dependant on the magnitude of the antenna voltage change. It also takes a period of time for the voltage level of the smoothing capacitor of the Auto-Tuner circuit to either rise or fall to the new measured voltage level.

Through observation, it was noted that consecutive jumper configurations do not result in a uniform change in antenna voltage magnitude. If the change in voltage level is relatively large, a waiting period must be inserted to achieve an accurate measurement of the voltage. If a relatively small change in voltage occurs for a particular jumper configuration, an accurate voltage measurement can be taken almost instantaneously.

Initially a standard waiting period of 1.5 s was inserted to account for these voltage transition periods. During testing it was found that this waiting period allowed for the accurate measurement of the voltage in all instances. This unfortunately made the execution time of the algorithm prohibitively long, as the waiting period of 1.5 s

must be applied for each of the 64 jumper configurations. This leads to an execution time in excess of 92 s for the measurement section of the algorithm alone.

To counteract this, a ripple detection algorithm was put in place. This algorithm detects if the voltage across the smoothing capacitor is changing following the change in antenna voltage magnitude. Firstly a shorter waiting period of approximately 150 ms is initiated. During this waiting period, the voltage across the smoothing capacitor is measured 10 times. If the lowest measurement taken is within 4% of the mean value of the 10 measurements, the transience is said to have ceased and the mean value found is taken as the measurement of the voltage for that particular jumper configuration.

If it is outside 4% of the mean level, another waiting period of 150 ms is initiated. This repeats for a maximum of 10 cycles, resulting in a total waiting period of a minimum of 1.5s. If after 1.5 s this condition is not met, the variation in the voltage measure is due to excessive voltage ripple on the smoothing capacitor. In this case the mean value found on the final cycle is taken as the voltage measure. Pseudo-code outlining the above operation is presented on the following page, with the final software code presented in Appendix A.2 of this thesis.

The final schematic of the Auto-Tuner circuit is shown in Appendix B.1 and the final Printed Circuit Board (PCB) of the design is shown in figure 5.5.

```
while ( i < 10 )
{
    //Loop repeated if voltage is still changing

    reset_timer1(10000); //Delay for transient
    voltage_mean = 0;
    voltage_min = voltage;
    k = 1;

    while ( k < 11 ) //mean
    {
        voltage_mean = voltage_mean + voltage;

        if (voltage < voltage_min) //find lowest
        voltage
            {
                voltage_min = voltage;
            }
        reset_timer1(100);
        wait_for_timer1();
        k = k+1;
    }
}
```

```

    }
    voltage_mean = voltage_max / 10;

    if ( (voltage_min * 1.04) > voltage_mean )
    //check for excessive ripple
    {
        i = 10;    //exit loop if low level of
ripple
    }
    i = i + 1; //Execute loop a maximum of 10 times
}

```

4.10 Optimum Antenna Voltage Initialisation

Once the system has cycled through each of the 64 possible jumper configurations and the array has been fully populated, the microcontroller initialises the jumper configuration stored in the first row of the array. This initiates the best possible capacitive impedance match with the loop antenna and results in the highest possible antenna voltage and current.

As outlined earlier, in certain instances it is undesirable to configure the antenna circuit to operate exactly in resonance and a jumper configuration resulting in a lower magnitude activation field may be desirable. To allow this a momentary switch connecting a 5V supply to an input pin of the microprocessor is used to step down through the 64 jumper configurations stored in the array in descending order. The initiation of each subsequent jumper configuration results in a lower antenna voltage/current.

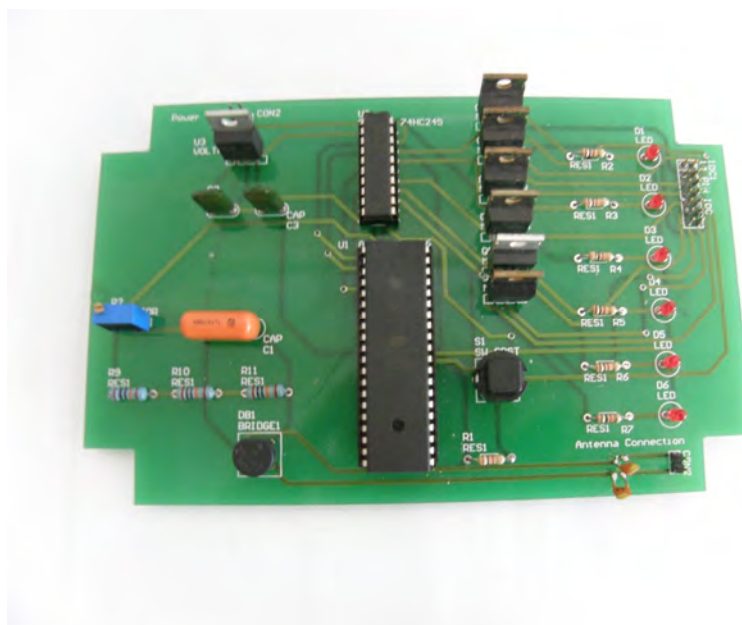


Figure 4.5: Auto-Tuner Printed Circuit Board

4.11 Auto-ID System Range Adjustment

It is a common requirement of an Auto-ID system to have control over the systems read-range. Therefore a system is required for the reduction of the activation field strength and read-range of an Auto-ID reader from the maximum levels. The most common method to achieve this is the de-tuning of the antenna circuit. This detuning ensures that the magnitude of the impedance of the inductive and capacitive elements no-longer match and therefore no-longer cancel out entirely. This increases the overall impedance of the antenna circuit, causing a reduction in the antenna current, the EM activation field and the resulting read-range.

While the de-tuning of the antenna circuit effectively reduces the EM field created by the RFID reader and hence reduces the read-range, it also reduces the level of tag backscatter received by the reader. As the antenna circuit is no-longer tuned to the frequency of the system operation (134.2 kHz) it can no-longer efficiently receive the tag signal at this frequency.

In an ideal situation, the read-range of a system is governed by strength of the EM field created by the reader to activate the Auto-ID tags and not the ability of the reader to receive the backscatter of the activated tag. In this situation the strongest possible backscattered signal is always received by the reader, reducing the probability of errors in reading the data stream from the tag. This reduces the effects of sporadic EMI on the operation of the system and ensures a more reliable read-range.

The activation of a tag is entirely dependent on the tag receiving suitable power from the EM activation field as described in section 2.2.2. Once the EM field results in the charging of the storage capacitor within the tag, the tag will respond (in accordance with the interrogation timing scheme outlined in ISO 11785 [1]) at a level defined by the tag construction.

$$H = \frac{I.N.R^2}{2\sqrt{(R^2 + x^2)^3}} \quad (4.6)$$

where, H is the magnetic field strength, I is the current in the antenna loop, N is the number of windings, R is the radius of the loop and x is the distance from the antenna

Equation 5.6 shows that the intensity of the EM field created by the reader antenna during activation is dependent on the current flowing in the antenna circuit at a given instant. Equation 5.2, presented earlier in this chapter, shows that this current value is directly proportional to the voltage level applied to the antenna circuit. Therefore the range within which activation of animal Auto-ID tags can be achieved is governed by the voltage of the waveform applied to the readers' resonant antenna circuit.

This section describes the development of a digitally controlled variable high-current low-cost power supply for use in a low-cost animal Auto-ID system. Such a power supply can be used within an automated tuning system for generation of an activation field of correct strength as required by the system.

4.12 Power Supply Requirements

This power supply must be able to vary its supplied voltage using a system which can be driven digitally from the I/O port of a microcontroller. It must also be capable of providing currents suitable for the operation of the EM interface of an Auto-ID system. The current required to drive the power stage of an Animal Auto-ID reader is characterised by a sine-wave current profile with maxima often in excess of 6 A, depending on the impedance of the antenna circuit. The system must also have a small footprint and remain relatively inexpensive as it will be used as a single component incorporated into an animal Auto-ID system.

4.13 Variable Voltage Source Circuit Design

A suitable variable power supply can be designed using a purpose built variable voltage regulator IC such as the LM338 [11]. The LM338 is a time-dependent current limited positive voltage regulator IC. This IC is capable of supplying a continuous 5 A of current at voltage levels of up to 32 V. It is also capable of supplying a peak current output of up to 12 A for a limited period of 0.5 ms.

A simple variable voltage source can be constructed using just the LM338 IC and two external resistors as shown in figure 4.6. This voltage regulator IC creates a constant voltage level, V_{REF} , between the V_{OUT} and ADJ terminals. In normal operation a V_{REF} of 1.25 V is created between these terminals. This voltage differential creates a current through the resistor R1 which in-turn must also flow through R2, as there is a high input resistance of the ADJ terminal. This current through R2 creates a voltage between the ground connection and the ADJ terminal in proportion to the current. The resulting V_{OUT} is equal to the sum of the voltage across R2 and V_{REF} .

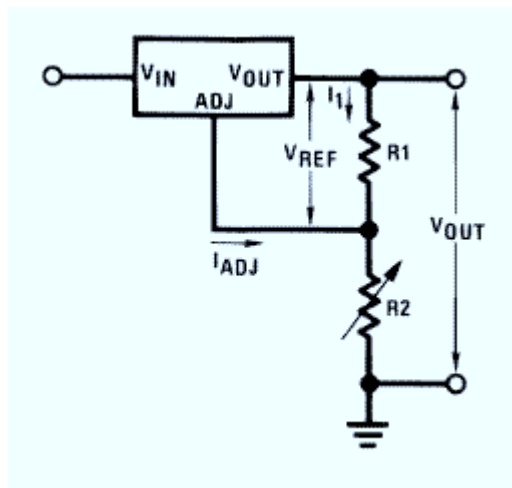


Figure 4.6: Variable Voltage Source using the LM338 [11]

Using the LM338 in this configuration, the output voltage (between V_{OUT} and GND) is governed by equation 4.7. Hence the output voltage can be controlled by varying the resistance R2.

$$V_{OUT} = V_{REF} \left(1 + \frac{R2}{R1} \right) + (I_{ADJ} \times R2) \quad (4.7)$$

A concern for this design is the magnitude of the resistance of R2. The LM338 datasheet lists the current I_{ADJ} as typically 45 μ A. If a large value of R2 is in the circuit, error term in the voltage equation ($I_{ADJ} \times R2$) becomes large. This will reduce the variability of the voltage supply. Therefore a maximum value for R2 was set at approximately 2 k Ω . This value would lead to an error of 90 mV.

Figure 5.9 shows the schematic used for the variable voltage source. The capacitor C1, placed between the voltage input and ground acts to reduce ripple on the voltage input line of the device. Capacitor C2 performs a similar ripple rejection operation on the voltage output line. Capacitor C3 is a protective element to prevent damage if the voltage output is momentarily connected to ground. In the case of this happening this capacitor provides the required current, but will only do so momentarily.

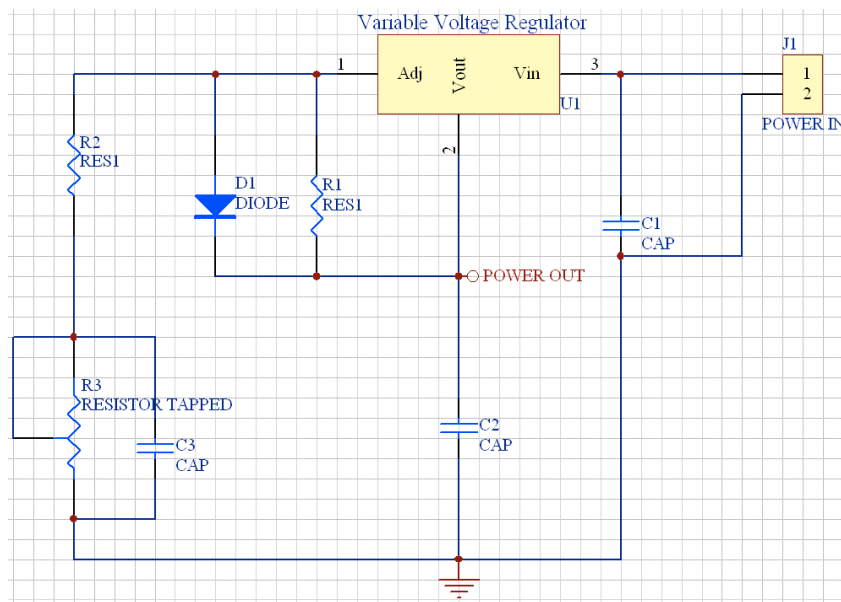


Figure 4.7: Digital Variable Voltage Source Circuit Schematic

The resistor R2 in figure 4.6 has been replaced by two resistors in series, R2 & R3, in figure 4.7.

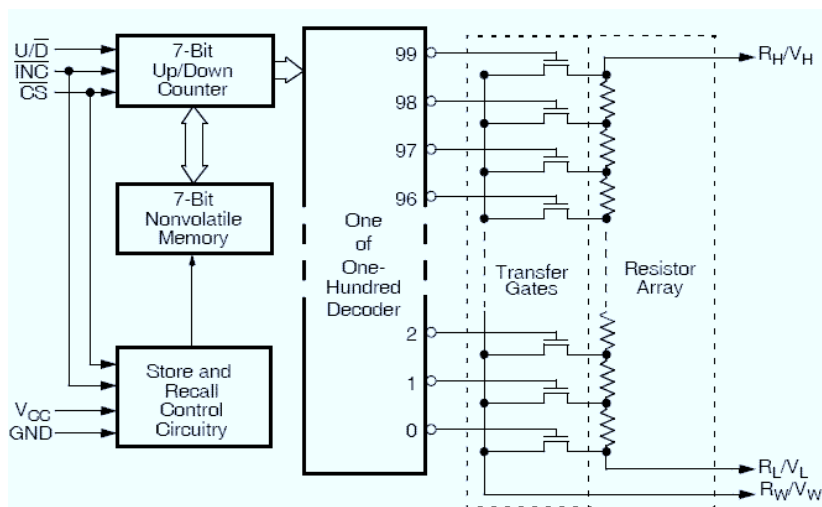


Figure 4.8: Block Diagram of X9C102 IC [12]

Resistor R3 takes the form of the Intersil[®] X9C102 [12], a 1000 Ω digitally controlled potentiometer. This device, whose components are shown in figure 4.8, consists of an array of 99 resistors, 100 wiper switches, a control section and a non-volatile memory location. The position of the wiper is controlled by a three-wire interface consisting of a Device Select, an Up/Down Select and an Increment. Such an interface can be easily operated by a microcontroller I/O port and allows the resistance value between the wiper and either of high or low resistor terminals to be varied from 0 Ω to 1000 Ω .

The maximum voltage which can be placed on the wiper terminal of this IC during operation is 5 V. This power supply must have the ability to supply up to 12 V. With a V_{REF} of 1.25 V, this would place 10.75 V on the wiper terminal of the potentiometer. Therefore a protective resistor is implemented in series with the 1k potentiometer. In the circuit diagram of figure 4.7, R2 fills this role. R2 must be chosen to provide the maximum voltage variation of the system while providing protection to the digitally controlled potentiometer. The calculation of a suitable value for the fixed resistance R2 is shown below.

$$V_{R2} + V_{R3_max} = 10.7V$$

$$V_{R2} = 10.7V - V_{R3_max} = 10.7 - 5 = 5.7$$

$$I_{R2} = I_{R3} = \frac{V_{R3_max}}{R3_{max}} = 5/1000 = 5mA$$

$$R_2 = \frac{V_{R2}}{I_{R2}} = \frac{5.7}{0.005} = 1140\Omega$$

$$R_1 = \frac{V_{REF}}{I_{R2}} = \frac{V_{REF}}{I_{R2}} = \frac{1.3}{0.005} = 260\Omega$$

Equation 4.7 has been altered to include the series resistors, R2 and R3, and is now shown in equation 4.8. In the following calculation the value of V_{REF} has been taken as its maximum value of 1.3 V to ensure the protection of R3 in all conditions.

$$V_{OUT} = V_{REF} \left(1 + \frac{R2 + R3}{R1} \right) + (I_{ADJ} \times (R2 + R3)) \quad (4.8)$$

The resulting maximum output voltage with the selected components is given below.

$$V_{OUT_MAX} = 1.3 \left(1 + \frac{1140 + 1000}{260} \right) + (45 \times 10^{-6} \times (1140 + 1000)) = 12.0963V$$

If the V_{IN} is 12 V this will be limited to a maximum of 12 V.

$$V_{OUT_MIN} = 1.3 \left(1 + \frac{1140 + 0}{260} \right) + (45 \times 10^{-6} \times (1140 + 0)) = 7.0513V$$

Under typical operating conditions, the value of V_{REF} will be 1.25 V resulting in an output voltage swing of 6.782 V to 11.634 V, as shown in the below calculations.

$$V_{OUT_MAX} = 1.25 \left(1 + \frac{1140 + 1000}{260} \right) + (45 \times 10^{-6} \times (1140 + 1000)) = 11.634V$$

$$V_{OUT_MIN} = 1.25 \left(1 + \frac{1140 + 0}{260} \right) + (45 \times 10^{-6} \times (1140 + 0)) = 6.782V$$

4.14 Microcontroller Control Interface

As described earlier, the output voltage level of the voltage regulator is controlled by the wiper position of the digitally controlled variable resistor. As the wiper position and hence the resistance value is controlled via a digital interface, this power supply can be controlled by the microcontroller through the digital interface of the variable resistor. To facilitate this, a suitable software program was created using the Processing programming language.

The control interface of the digital potentiometer consists of a 3-wire serial interface comprising of a Device Select pin, an Up/Down Select pin and an Increment

pin. The IC is active when the device select pin is connected to a low signal. The position of the closed wiper switch terminal is controlled by the Up/Down Select and the Increment pins.

A 7-bit up/down counter controls the position of the closed wiper switch. The number present on this counter is then decoded using a one-to-one-hundred decoder resulting in the closing of a single wiper terminal switch. The incrementing of this up/down counter is falling edge triggered, therefore when an increment of the counter is required a pulse must be applied to the Increment pin of the IC. The direction of the increment is controlled by the level present on the Up/Down pin on the falling edge of the Increment pin. A high level will result in the incrementing of the counter, while a low level will result in the decrementing.

For demonstration purposes, this digitally controlled power supply will be operated using a dual push-button system, one button to increase the output voltage and the other to decrease it. When incorporated into an Auto-ID system control could come directly from the control algorithm in place on the Auto-ID control board, based on the inputs received from a series of sensors or instructions received from the user.

As shown earlier, the power supply output voltage level can be altered from 6.782 V to 11.634 V. Using the X9C102 digital potentiometer the voltage will have 1000 intermediary values between these voltage levels, giving a resolution of 4.85 mV. For practical application in an Auto-ID system this resolution is excessively fine, especially as an option to manually alter the voltage level via a push-button system is available. This would mean 1000 button-pushes to bring the output voltage from maximum to minimum. To counteract this, the microcontroller implements a series of 10 pulses to the Increment pin per button push. For implementations where the voltage source is being controlled solely by an automated read-range adjustment algorithm, this feature would not be necessary. The final circuit diagram is shown in figure 4.9 and in Appendix B.2. Figure 4.10 shows the fully functioning prototype digitally controlled variable voltage source. The final Processing coded program can be found in Appendix A.4.

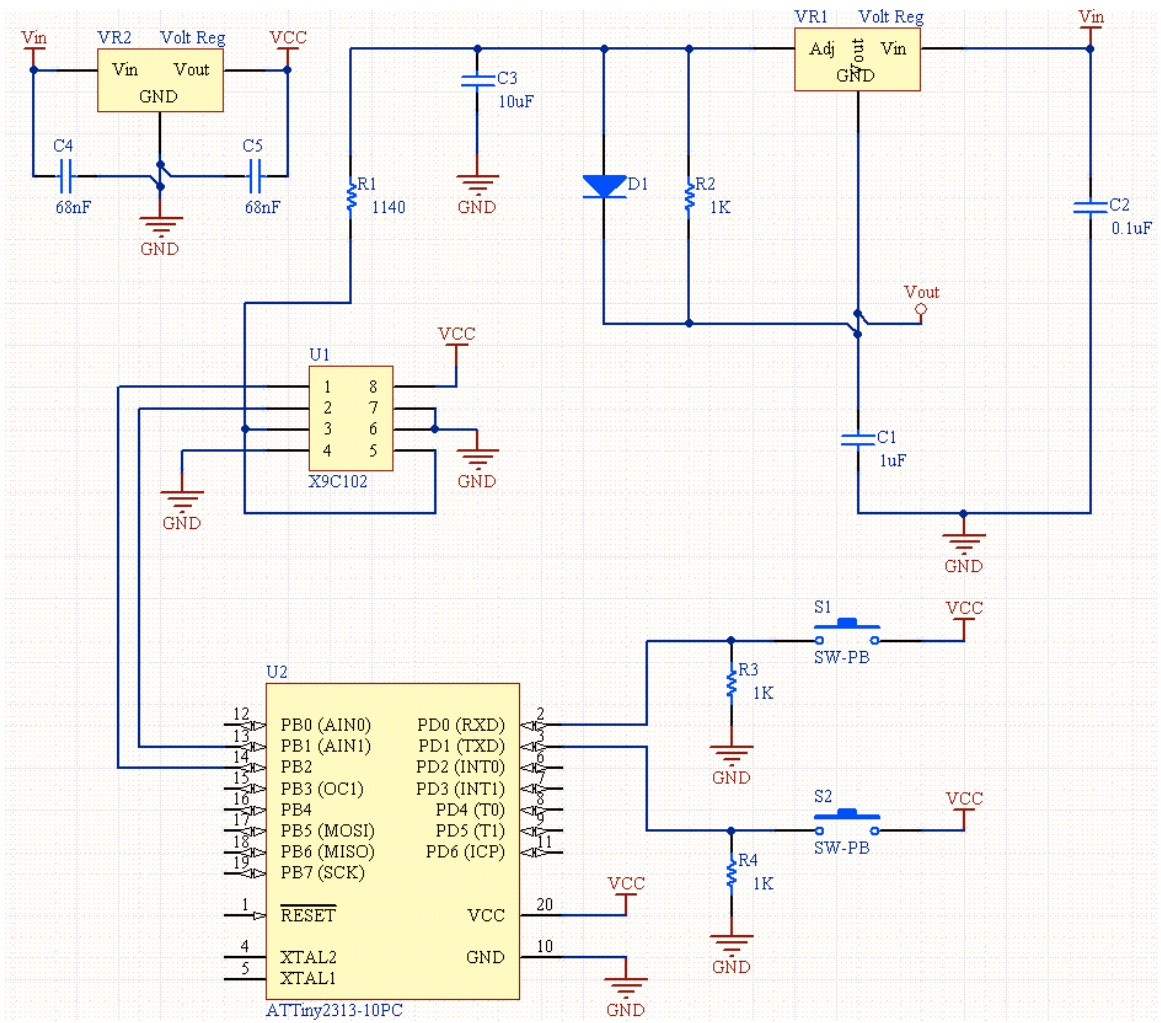


Figure 4.9: Final Digital Variable Voltage Source Circuit Schematic

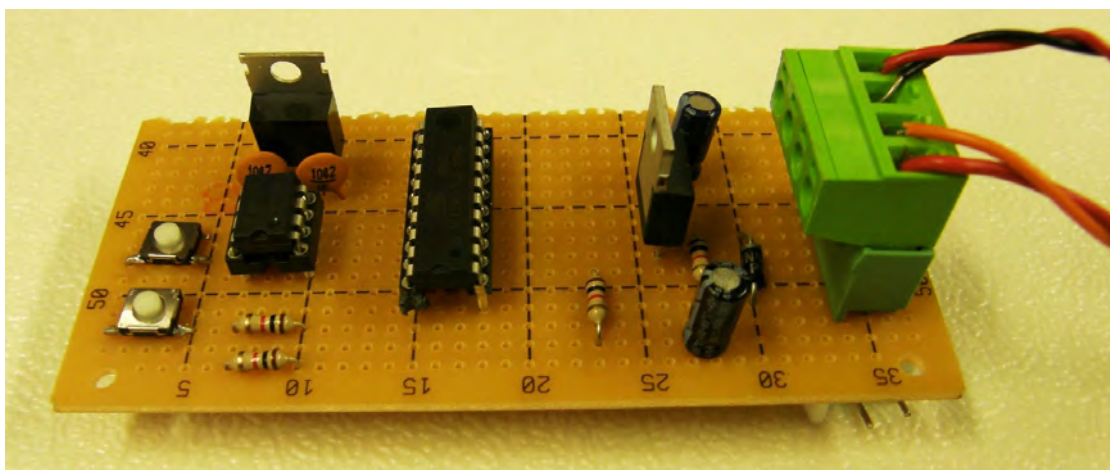


Figure 4.10: Prototype Digitally Controlled Variable Voltage Source

4.15 Results and Conclusion

This chapter has described the development of a device for the automatic tuning of the antenna circuit of an animal Auto-ID reader. The resulting auto-tuning device has eliminated the need for the manual reconfiguring of the tuning capacitor jumpers and subsequent voltage measurements during the antenna circuit tuning process. Upon completion of the auto-tuning process the jumper configuration resulting in the optimum operation of the antenna circuit is applied to the capacitive bank via the auto-tuner MOSFETs. It is also possible for the auto-tuner to step down through the various capacitor bank jumper configurations which have been ordered in accordance with the antenna voltage level they produced during the tuning process.

Once the auto-tuning process has suitably tuned the antenna circuit of the reader, it can be either left attached to the reader or removed from the system. If it is removed, jumper connections which had been made by the MOSFETs of the auto-tuner must be replaced by jumper pins. The location of these jumper connections is indicated by the auto-tuners LED's. An activated LED indicates a MOSFET in an 'on' state. Jumper pins must be inserted to replace all 'on' MOSFETs.

While this resonant antenna auto-tuning process has been designed specifically for operation with the Texas Instruments[®] Auto-ID module, the basic principle can be applied to any system which requires the capacitive tuning of an RLC circuit desired to operate in resonance. Such systems include tuned filters for use in analogue communications receivers.

This chapter has also described the development of a digitally controlled voltage source suitable for use with an animal Auto-ID reader. The resulting power supply has the ability to supply voltage levels in the range 6.782 V to 11.634 V with a resolution of 4.85 mV. This voltage level can be controlled through a digital interface using a microcontroller which will allow for the future automation of read range adjustment of an Auto-ID reader. This variable power supply is capable of supplying a current of 5 A continuously with pulses of up to 12 A over a short period of time.

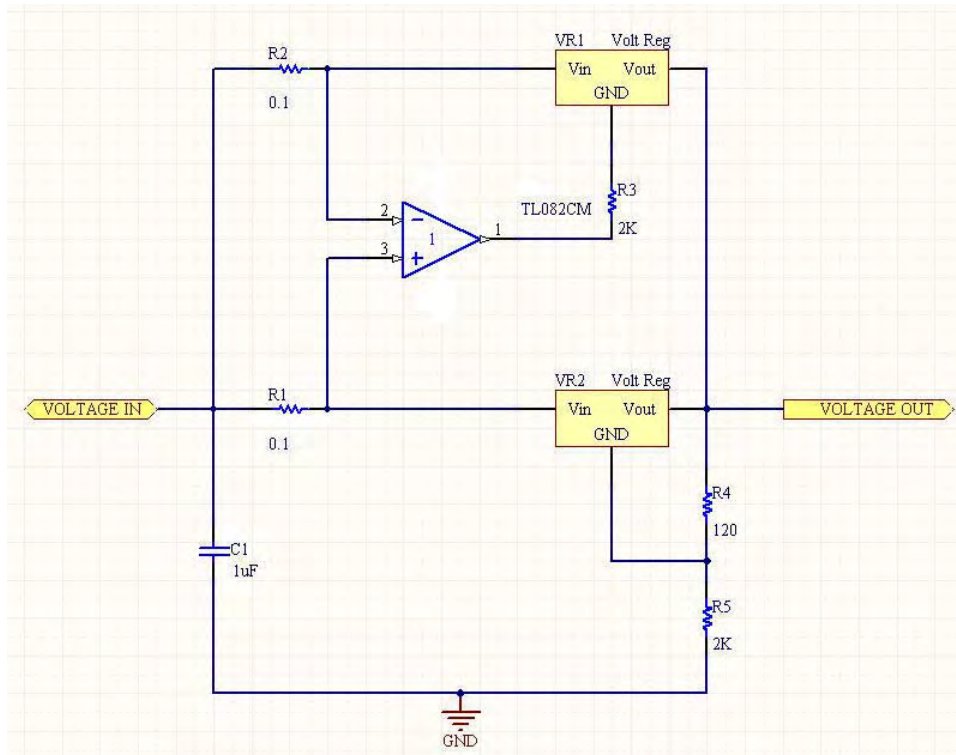


Figure 4.11: 10 A Variable-Voltage Regulator

If currents of larger magnitudes are required a second LM338 IC can be added to the design as shown in figure 4.11. An op-amp is used to ensure that the current supplied by the voltage regulator is shared equally by the two LM338 ICs [11]. The voltage can be varied, as before, by replace the resistor R2 by an X9C102 digitally controlled variable resistor and a protection resistor.

4.16 References

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Chapter 5

Case Study 2: A Low-Cost Animal Auto-ID Reader

5.1 Introduction

As described in detail in chapter 3, animal Auto-ID systems are vital in the current climate of increased animal traceability and farm automation requirements. The use of Auto-ID systems within dairy farms allows the automation of the processes of animal drafting, weighing, health-monitoring and feeding, among others. At present Dairymaster[®] use a Half Duplex (HDX) based animal Auto-ID system as an integral part of their dairy parlour automation system. The Dairymaster[®] Animal Auto-ID system is built around a Texas Instruments[®] Series 2000 RFID module [1], conforming to I.S.O. standards 11784:1996 and 11785:1996 [2, 3].

While the current system is very effective in the automatic identification of animals, leading to a high level of dairy parlour automation, cost often proves to be a limiting factor in the scale to which this Auto-ID system is implemented. In addition, when presence of electromagnetic interference (EMI) reduces the read-rate of an animal Auto-ID system ‘missed-reads’ may occur. By increasing the number of Auto-ID readers in a facility, the probability of a ‘missed’ animal entering the parlour is reduced. The development of a low-cost animal Auto-ID reader would allow the placement of Auto-ID readers in additional locations throughout the dairy parlour, allowing greater and more reliable levels of parlour automation and animal traceability.

This case study describes the development of a low-cost animal Auto-ID reader module which will integrate with the current Dairymaster[®] Auto-ID system. Firstly a description of the current Dairymaster[®] Auto-ID system control board will be presented. Then the requirements of the Auto-ID module to be developed will be outlined, followed by a description of the functionality of the basestation integrated circuit (IC) around which the reader is to be designed. The case study will continue with the development of a power amplification stage required to drive a resonant

resistive-inductive-capacitive (RLC) antenna circuit, a suitable antenna circuit and a suitable signal filtering stage to remove interference from the received signal to be demodulated. Finally, the resulting HDX Auto-ID reader module will be tested and evaluated.

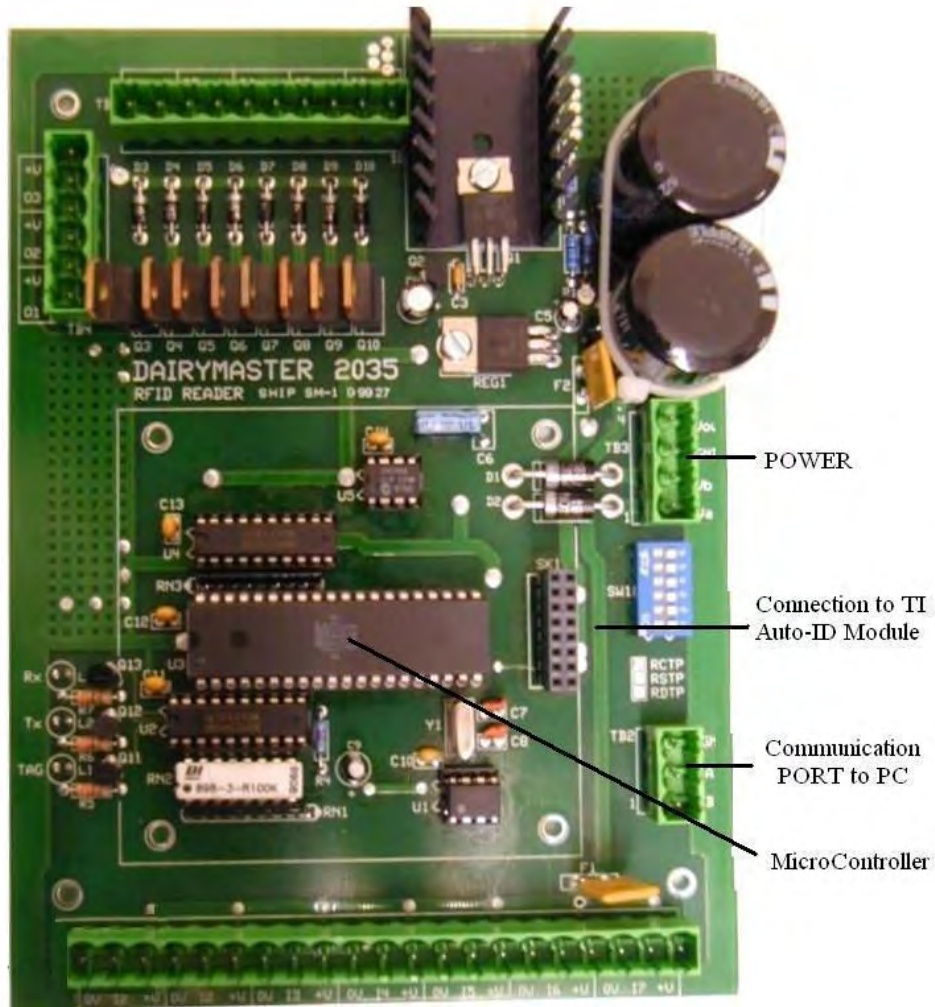


Figure 5.1: Dairymaster[®] Auto-ID System Control Board

5.2 Dairymaster[®] Auto-ID Control System

The Dairymaster[®] Auto-ID Control Board, shown in figure 5.1, provides power and control for the Texas Instruments[®] HDX Auto-ID module. It also provides an interface between the Auto-ID module and a PC hosting the herd management and parlour automation software. The control board provides a regulated and current limited 12 V supply line to the Auto-ID module. The triggering of the reader's HDX

activation period and listening period, in accordance with the I.S.O. standards, is achieved by a 5 V squarewave provided to the control section Auto-ID module.

The reception and demodulation of the Auto-ID tag response by the Auto-ID module results in a bit stream containing a tag header, a unique animal ID code and a Cyclic Redundancy Check (CRC) error detection code. The Dairymaster[®] Auto-ID Control Board receives this demodulated bit stream, performs an error detection routine using the CRC code and, if the bit-stream is free from error, the unique animal ID code is transmitted to the PC for use within the farm automation system.

5.3 System Requirements

The main requirement of the developed low-cost Animal Auto-ID module was that it successfully interrogates HDX animal Auto-ID tags in accordance with ISO standard 11784 and 11785 [2, 3]. These standards specify that both FDX and HDX Auto-ID transponders can be read using a single transceiver system. As the Texas Instruments[®] Auto-ID module and the current Dairymaster[®] system only operate with HDX Auto-ID tags, the device developed here will concentrate on the reading of HDX tags, to allow the direct replacement of this module. It is also required that this newly developed Auto-ID module integrates with the current Dairymaster[®] Auto-ID control system.

The activation of these tags is accomplished through the use of an electromagnetic (EM) activation field of frequency $134.2(\pm 13.42)$ kHz and of suitable strength to energize an animal Auto-ID tags appropriately. To facilitate the activation of HDX tags, an activation period of 50 ms is specified. Upon completion of the 50 ms activation period, the 134.2 kHz activation signal is then ceased. It is also specified by the ISO standards that the activation field must drop from -3 dB to -80 dB within a period of 1 ms. If a HDX tag is present within the read-range of the system, it will respond within 3 ms of the dropping of the activation field. This response is a Frequency Shift Key (FSK) modulated signal which must be demodulated by the reader in real-time. The resulting bit-stream must then be transmitted from the reader and made available to the next component of the Auto-ID system.

5.4 The RI45538 Low Frequency RFID Basestation IC

The Texas Instruments® RI45538 IC [4] is an Application Specific Integrated Circuit (ASIC) designed for the activation of low frequency (LF) HDX Auto-ID tags and the reception, filtering and demodulation of the subsequent FSK tag data signal.

As can be seen in figure 5.2, the IC is divided into a number of blocks. A logic control section synchronises the operation of the blocks of the IC. This ensures that the demodulation and transmit sections operate in accordance with the timing schedule and at the correct frequency as outlined in the I.S.O. standard. The transmit block takes input from an external crystal oscillator and from this signal generates the activation signal at 134.2 kHz. This is then fed to the activation signal output terminals via two low-power MOSFETs in a push-pull configuration. The demodulation section performs a FSK demodulation of the amplified and filtered signal which has been returned from an activated tag.

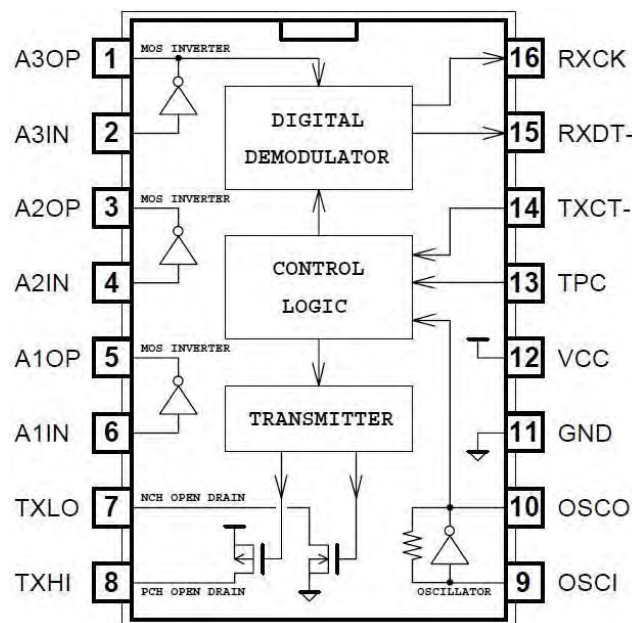


Figure 5.2: Block Diagram of RI45538 I.C. [4]

The demodulator in this IC operates only as a FSK demodulator. Also the transmit section and demodulator are activated by opposite voltage levels applied to the TXCT- pin of the IC and, hence, cannot operate simultaneously. Therefore an Auto-ID reader built around this I.C. can only conform to the section of the I.S.O. standards detailing the interrogation of HDX animal Auto-ID tags.

The RI45538 IC requires a regulated power supply of 5 V and Ground, applied to pins 12 and 11 respectively. A crystal oscillator of frequency 17.116 MHz is required to generate the activation of signal of 134.2 kHz. This is achieved through an on-chip frequency division of 128. On the positive cycle of the control signal, presented to TXCT-, the 134.2 kHz activation signal is output on pins 7 and 8 of the IC. These outputs are designed to provide power to a small, low Q antenna circuit. The IC provides 3 high gain invertors for the purpose of amplifying and filtering the signal received from the tag under interrogation. A series of external passive components are required to construct these filters. The final input to the ICs internal demodulator is on pin 1.

Once the signal supplied to the RI45538 IC is filtered, amplified and demodulated, the resulting bit-stream is output on pin 15, RXDT-. This bit-stream is synchronised with a data clock signal generated by the IC and output on pin 16, RXCK.

5.5 Circuit Design

This module is based around the Texas Instruments® RI45538 LF RFID basestation IC described in section 6.4. In addition to this IC, this circuit design requires a power supply, a control section, a high-power transmit stage, an antenna circuit and a signal return path for HDX tag signal. This module will be connected to the DairyMaster® Auto-ID Control Board via the existing connection used to connect the Texas Instruments® Auto-ID module.

5.5.1 Power Supply

A 5V power supply is required to power the RI45538 RFID basestation IC and various other ICs in this circuit design. Surface Mount Technology (SMT) ICs can be very sensitive to supply fluctuations; therefore a voltage regulator is required between the device power supply and the ICs. A 5 V linear voltage regulator is used in this design, along with suitable ripple rejection circuitry.

As shown in Case Study 1, the magnitude of the EM field created by the antenna driver circuit of an Auto-ID reader is directly proportional to the voltage supplied to

the circuit. Therefore, it is beneficial for the antenna driver circuit of this design to be supplied with a power supply capable of supplying larger voltage at large current values. This will allow a larger magnitude of antenna current and voltage, hence increasing the magnitude of the EM activation field and increasing the read-range of the device. Therefore the maximum voltage available from the Dairymaster[®] control board, 12 V, is used as the supply voltage of the transmission stage of this Auto-ID module. Future revisions of the Dairymaster[®] Auto-ID control board may include the digitally controlled variable voltage supply designed in Case Study 1.

5.5.2 Control Section

A 17.1776 MHz crystal is required for the generation of the activation signal at 134.2 kHz. This specific value is required to allow the simple frequency division of the crystal oscillator waveform by 128, resulting in a 134.2 kHz signal. It is specified by the I.S.O. standards that the activation signal should be transmitted for a period of 50 ms to allowing the charging of capacitor of any tag within range. This 50 ms activation period is to be followed by 20 ms within which the reader is in listening mode. This results in a total duty cycle of 70 ms. To control these intervals the RI45538 IC requires an externally generated 5 V 14.28 Hz squarewave with suitable pulse-widths, to be provided from the Dairymaster[®] Auto-ID control board. On the low stage (0 V) of this squarewave the I.C. generates the activation signal and deactivates the FSK demodulation section. On the high stage (5 V), the activation signal is terminated and the demodulation section is activated.

Initially it proved difficult to source a 17.1776 MHz crystal oscillator for the generation of the 134.2 kHz signal, as it not a common oscillator value. Until a suitable oscillator could be sourced, a programmable crystal oscillator was used. The Cardinal[®] PG-3000 Field Instantly Programmable Oscillators (FIPO) programmer system [5] was used. This has the ability to program the frequency (1 – 133 MHz), voltage (2.7 V, 3.3 V, and 5 V), output control (synchronous or asynchronous), tri-state (enable or power-down), and CMOS, TTL, LVDS, and LVPECL logic levels of a Cardinal blank oscillator. A Cardinal[®] oscillator programmed to 17.1776 MHz with a voltage of 5 V and a stability of 25 part per million. This oscillator produced the required 17.1776 MHz oscillating signal to the RI45538.

In the final design, this was replaced with a purpose built crystal oscillator of frequency 17.1776 MHz.

5.5.3 Transmit Stage

The internal transmit stage of the RI43358 IC is designed for very low power applications with extremely limited read-ranges. For higher power applications with extended read-ranges, an external power amplification stage consisting of high-power MOSFETs in a push-pull configuration. This external power stage will be driven using the output of the internal IC transmit stage.

A push-pull power-stage consists of a P-channel and an N-channel MOSFET connected in series as shown in figure 5.3. Here, the source of the N-channel MOSFET is connected to ground while the source of the P-channel MOSFET is connected to the positive voltage supply rail of 12 V. The Drain pins of the P-Channel and the N-Channel MOSFETs are connected together. This configuration allows a single 12 V_{p-p} squarewave to operate both MOSFETs of the amplifier. On the positive cycle of the squarewave, the N-channel MOSFET turns on while the P-channel turns off, providing the output with a low-impedance connection to ground. On the low-cycle of the squarewave the N-channel turns off while the P-channel turns on, providing the output with a low-impedance connection to the 12 V supply line. The MOSFETs used in the push-pull stage must have a low on-impedance and the ability to conduct large currents at maximum voltage of 12 V. The MOSFETs IRF540 [6] and IRF5210 [7] were chosen.

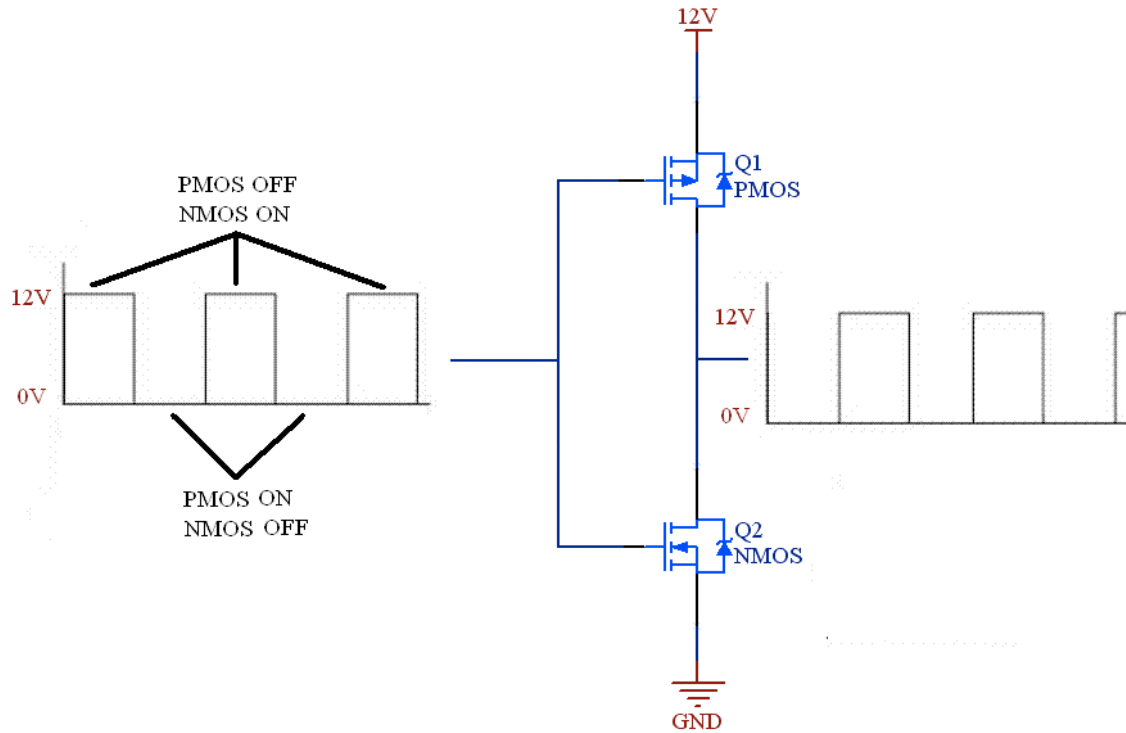


Figure 5.3: Push-Pull Amplifier Operation

The output of the RI45538 IC activation signal generation block is a 5 Vp-p squarewave at frequency of 134.2 kHz. As outlined earlier a 12 Vp-p signal is needed for the operation of the push-pull circuit as the source of the P-channel MOSFET is referenced to the 12 V power line.

To convert the 5V squarewave activation signal created by the RI45528 to a 12 V squarewave signal for the control of the push-pull amplification stage an NXP[®] HEF4104 [8] voltage translator IC was used. Upon testing it was found that the translator was not capable of providing enough current to effectively drive the input capacitance of the high-power MOSFETs at a frequency of 134.2 kHz. The input capacitance of the IRF540 N-channel MOSFET is rated at 1960 pF while the IRF5210 P-channel MOSFET is rated as 2700 pF. This resulted in a slow turn-on/off time of the MOSFETs, again resulting in excessive current flow through the P-channel MOSFET. The charge required to drive the input of the P-Channel MOSFET is given by equation 5.1 and 5.2. From equation 5.1 it can be seen that by increasing the current available to the input of the MOSFET, the switching time can be reduce.

$$Q = C \cdot V = I \cdot T \quad (5.1)$$

where Q is the charge required to raise the voltage across the input capacitance, C , to the level, V , I is the current provided to the input of the MOSFET and T is time to raise the input by the desired voltage level.

$$Q = 2700 \times 10^{-12} \cdot 12 = 32.4 \times 10^{-9} \text{ C} \quad (5.2)$$

To provide more current for the switching of the high-power MOSFETs of the push-pull circuit, an intermediary push-pull configuration circuit was used. This circuit was comprised of low/medium power MOSFETs with a low input capacitance, allowing for faster switching when driven by the 12V voltage translator. The Fairchild Semiconductor[®] FDY100PZ [9] with an input capacitance of 100 pF and the Fairchild Semiconductor[®] BSS138 [10] with an input capacitance of 27 pF were chosen. This dual cascade style push-pull circuit is shown in figure 5.4.

The push-pull amplification provides a 134.2 kHz squarewave of amplitude 12 V to the resonant antenna circuit during the activation cycle. The driving waveform is shown in figure 5.5.

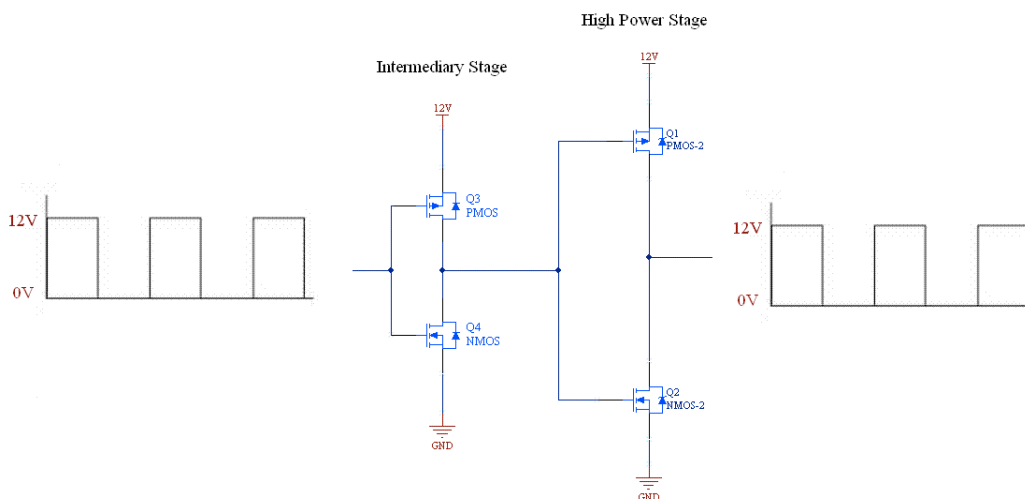


Figure 5.4: Cascade Push-Pull Amplifier Configuration

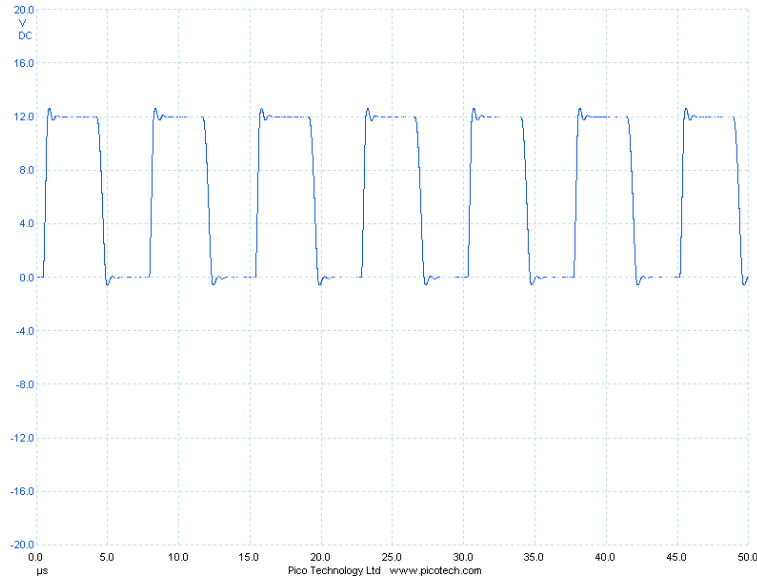


Figure 5.5: Antenna Circuit Driver Waveform

5.5.4 Antenna Circuit

In order for this LF Auto-ID reader module to activate passive HDX Auto-ID tags, the system must generate an EM activation field of suitable strength at the specified frequency of 134.2 kHz. This is best achieved when the antenna circuit of the system is resonant at this specified frequency. This antenna circuit must also be able to receive the backscattered response from the Auto-ID tags. The antenna circuit will take the form of a loop antenna circuit, which can be thought of as an inductance (L), and a capacitance (C) connected in series.

The equation to calculate the resonant frequency (f_r) of an LC circuit is shown in equation 6.3.

$$f_R = \frac{1}{2\pi\sqrt{LC}} \quad (5.3)$$

It is required that this antenna circuit resonates at a frequency of 134.2 kHz and a standard Dairymaster[®] Auto-ID antenna of inductance 26µH will be used. Therefore, in accordance with equation 5.3, a tuning capacitance of 52.1 nF is required to make the circuit resonate at the desired frequency. Testing has shown that, in the presence of objects of high permeability such as metals, the inductance of such an air-core loop antenna can change by as much as 15%. For this reason, the tuning capacitance must

be variable in the field. To allow for this an array of six tuning capacitors are provided.

In a resonant RLC circuit the complex impedances due to the inductance and the capacitance of the circuit cancel each other out, as they are equal in magnitude but 180° out of phase. Therefore the circuit impedance is composed entirely of its Ohmic resistance. The current in the antenna circuit can then be calculated as shown in equation 5.4.

$$I_{MAX} = \frac{V_{CC}}{R_{OHMIC}} \quad (5.4)$$

The maximum voltage value on the antenna can then be calculated from equation 5.5

$$V_{MAX_ANTENNA} = X_L \times I_{MAX} \quad (5.5)$$

where, $X_L = 2\pi fL$

In practice, the ohmic impedance of an Auto-ID antenna is in the region of 100 to 200 mΩ but other components of the antenna drive circuitry, in particular the MOSFETs and the circuit routing, raise the effective impedance of the antenna circuit to approximately 1Ω. The voltage applied to the antenna circuit is 12 V. This yields an I_{MAX} of 12 Amps.

$$P = RI^2 = 0.1 \times 12^2 = 14.4W \quad (5.6)$$

For a power MOSFET with ‘On Resistance’ of 0.1 Ω, this yields power dissipation in the region of 14.4W as shown in equation 5.6. Dissipating this level of power in each of the push/pull MOSFETs of the output stage will lead to issues regarding the reliability and the heat dissipation requirements of the circuit. Issues also arise with the power supply module of the system, as DairyMaster® do not currently use a power supply capable of providing a DC current of 12 A at 12 V. For these reasons an alternative antenna circuit was needed which could be driven effectively while requiring less current to pass through the output stage MOSFETs.

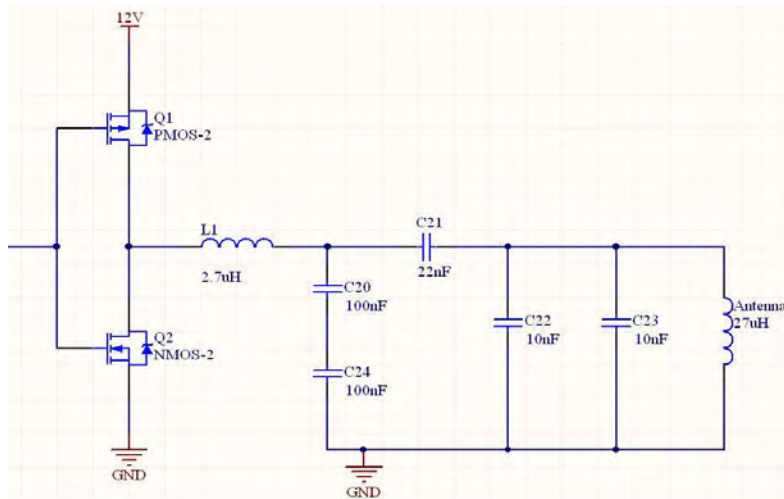


Figure 5.6: Cascade Resonant Antenna Circuit

An antenna circuit using cascading resonant circuits, shown in figure 5.5, was implemented, which uses a low Q series RLC circuit (composed of inductor L1 and capacitors C20 and C24) to drive a second high Q resonant parallel LC circuit (capacitors C21, C22 and C23 and the loop antenna). This circuit configuration allows the push-pull MOSFET circuit to drive the high current resonant antenna circuit, while switching only one sixth of the required antenna current. [11]

Loop Antenna Design

The activation of an Auto-ID tag is dependent on the required amount of energy being harvested by the tag from the EM activation. Energy transfer in the LF domain operates predominantly in the near-field region through mutual magnetic inductance, as described in section 2.2.2.

Mutual inductance is the generation of a voltage on one conductor due to the presence of a current in another conductor. The equation for the mutual inductance between two air-core loops of conducting wire (with one loop being considerable larger than the other) can be derived directly from Biot-Savarts law [12]:

$$B = \frac{\mu_0}{4\pi} \int \frac{Idl \times \hat{r}}{r^2}$$

$$\begin{aligned}
B &= \frac{\mu_0}{4\pi} \int \frac{Idl \times a}{|a^2 + h^2|^{\frac{3}{2}}} \\
\int dl &= 2\pi a \\
B &= \frac{\mu_0 I a^2}{2|a^2 + h^2|^{\frac{3}{2}}} \\
M &= \frac{\phi_2}{I} = \frac{BA}{I} = \frac{B\pi x^2}{I} = \frac{\pi\mu_0 a^2 x^2}{2\sqrt{(a^2 + h^2)^3}} \quad (5.7)
\end{aligned}$$

Where: a is the radius of the larger coil

x radius of the smaller coil

h is the distance between the coils

ϕ_2 is the flux through the smaller loop

μ_0 is the permeability of free space

B is the Magnetic Field Strength

A is the area of the loop

I is the current flowing in the loop

Assuming very tightly wound conductive coils with multiple windings, the mutual inductance can be calculated from:

$$M = N_1 N_2 M_0 \quad (5.8) \quad [13]$$

where N_1 and N_2 are the numbers of winding in each coil and M_0 is the mutual inductance if each coil only had a single winding as in equation 6.7. Therefore the mutual inductance between two coils of wire, similar to the reader and tag antennas in question here, is proportional to the number of windings in each and the radius of the coils. By increasing the mutual inductance between the reader antenna and the tag coil the levels of energy received by the tag can be increased, hence increasing the read-range of the system.

The current Dairymaster[®] Auto-ID system loop antenna consists of a rectangular coil of wire of dimensions 0.55 m by 1m with three windings. This results in an inductance of approximately 26 uH. To increase the mutual inductance of the system a new antenna was designed. It is possible to increase the mutual inductance of a system by increasing either the dimensions or the number of windings of the coil. As it was desirable for this projects industrial partner that the dimensions of the antenna remain unchanged, the number of winding in the coil was increased to 6. This increased the inductance of the antenna to 118.5 uH. Once this antenna was connected and the antenna circuit was successfully tuned the read-range of the system increased to approximately 1.1 m due to the increased coupling of the reader and tag antennas.

During testing it was found that the higher inductance antenna was more susceptible to changes in its inductance value due to the presence of external objects of high permeability. Dairymaster[®] Auto-ID antennas are placed in an agricultural setting on drafting gates as shown in figure 3.5, contained in chapter 3. These drafting gates are constructed almost entirely of steel. Steel has a permeability of approximately 700 times that of air and therefore has a large effect on the inductance of the antenna loop. This is described in greater detail in section 4.4. Testing showed that the 26 uH antenna loops inductance varied by approximately 15%, while the 118.5 uH loop varied by approximately 25%. Therefore this antenna loop will need a wider variation in the tuning capacitance of the antenna circuit, leading to less accuracy in the tuning process. Taking this into account and the economic and logistical benefits of using the existing antenna design, it was decided by Dairymaster[®] that this device should operate with the existing 26uH loop antenna.

Dynamic Antenna Circuit Retuning

When operating an antenna circuit of high Q value, the frequency response of the antenna circuit is of great importance. A high Q factor means a sharp peak in the frequency response at the frequency of resonance, while a lower Q factor results in a more smoothed peak.

$$Q = \frac{X_L}{R} = \frac{1}{R} \sqrt{\frac{L}{C}} \quad (5.9) \quad B = \frac{f_0}{Q} \quad (5.10)$$

Equations 5.9 and 5.10 show that as the Q factor of the antenna circuit increases as the bandwidth of the receive circuit decreases. At a high Q value, when the antenna circuit is tuned for the transmission of a 134.2 kHz signal, it becomes inefficient for the reception of the 124.2 kHz portion of the FSK tag response signal.

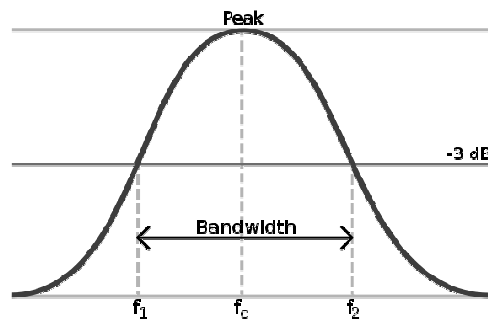


Figure 5.7: Antenna Circuit Bandwidth (Frequency versus Magnitude)

To allow for the use of a high-Q antenna during activation field generation, a system of dynamic antenna circuit retuning is implemented. By utilising the activation signal control waveform to control a high voltage, low on-resistance MOSFET the inclusion and exclusion of a retuning capacitor can be achieved. By choosing the correct capacitance value to be added to the antenna circuit during the readers listening period, the antenna circuit can be retuned to resonate at a frequency of 129.2 kHz, allowing for the reception of both frequency values of the HDX Auto-ID tag response with almost equal antenna circuit gain.

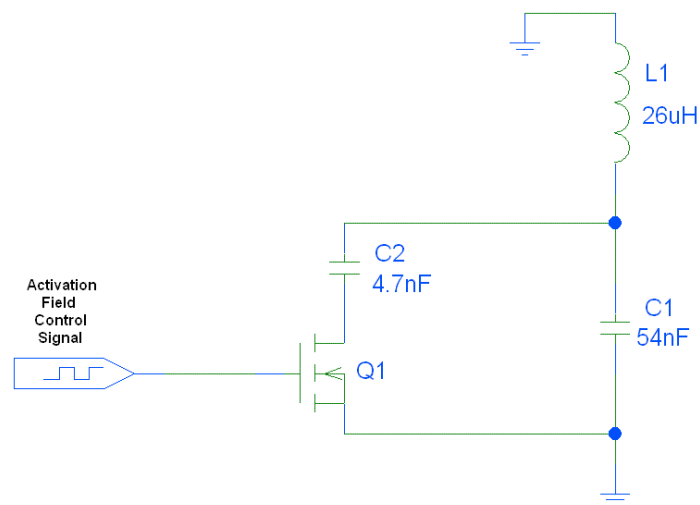


Figure 5.8: Dynamic Antenna Retuning Circuit Schematic

The antenna circuit antenna circuit to be used in this design is comprised of a 26 uH loop antenna along with a 54.1 nF tuning capacitor. In accordance with equation 5.3, to tune an antenna circuit containing a 26 uH antenna to resonate at 129.2 kHz, a capacitance of 58.36 nF is needed. Therefore the addition of approximately 4.2 nF to the capacitive element of the antenna circuit is required. To allow for the use of standard capacitor values a 4.7 nF capacitor is used, as in figure 5.8.

5.5.5 HDX Signal Return Path

Firstly the signal presented to the signal return path from the antenna circuit must be limited to approximately 5 V to allow the safe manipulation of the signal with standard components. This is achieved using two clamping diodes, with one connected in forward bias to the 5 V power rail and the other connected in reverse bias to the ground power rails. This serves to protect the data capture system from the excessive voltage levels that may be present on the antenna during the activation period. When the voltage on the antenna line becomes greater than 5 V, the first diode enters forward bias, effectively connecting the antenna line to the 5 V power line. When the antenna voltage drops below the 0V (ground), the second diode becomes forward biased connecting the antenna line to ground and hence limiting the lower level of the antenna voltage. A 1 nF capacitor is used to isolate this reduced voltage level from the high-voltage signal on the antenna.

The return path of the RI45538 IC contains a number of inverters and comparators to be used to amplify the received signal and create a band-pass filter to remove EMI from the signal using external components. Using a series of capacitors and resistors connected as shown in figure 6.11, a band-pass filter of centre frequency 130 kHz is created to ensure any noise which has been added to the signal received from the HDX tag will be removed before demodulation. The details of this filter are supplied in the RI45538 IC datasheet [4].

5.5.6 HDX Demodulation and Data Stream Return

Once filtered and amplified the waveform is FSK demodulated by the Digital Demodulator block of the RI45538 IC. The resulting bit-stream is output on the RXDT pin of the IC. This output is synchronised with the clock signal which is present on pin RXCK of the IC. The bit-stream and synchro-clock signal are then sent

to the DairyMaster[®] Auto-ID control board for CRC error detection and subsequent processing and/or transmission to a host PC for use within the herd management software.

5.6 Results and Discussion

Testing was carried out using the experimental setup described in section 8.2.1 with a DairyMaster[®] portal antenna. It was immediately discovered that the HDX bit-stream returned to DairyMaster[®] control board was inverted with respect to the bit-stream generated by the Texas Instruments[®] RFID module. A simple software change within the DairyMaster[®] Auto-ID control board to invert the bit-stream signal solved this issue.

Upon testing, the Auto-ID reader developed here performed as designed and had the ability to successfully activate and received the signal transmitted by HDX animal Auto-ID tags. The reader could then filter and amplify the received signal and subsequently FSK demodulate the HDX signal and output the resulting bit-stream. The full schematic of the design is contained in Appendix A.5. The completed reader module is shown in figure 5.9.

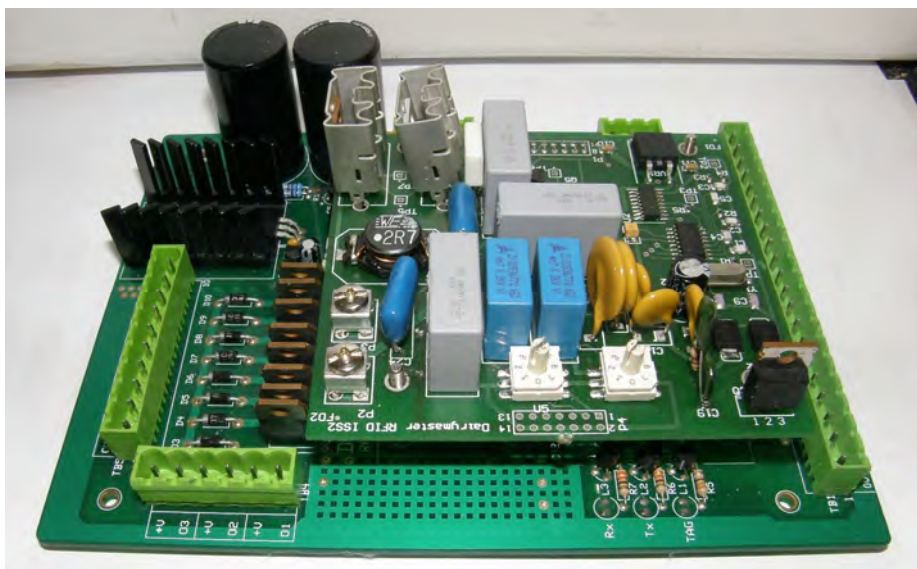


Figure 5.9: Complete Reader Module

It was found that the reader could perform with a range of up to 1 m in low EMI conditions for HDX animal Auto-ID tags. When EMI in the region of 100 – 160 kHz was introduced range was reduced considerably, as expected, in accordance with the magnitude of the EMI. A screen-grab of the demodulated bit-stream is shown in figure 5.10.

Through analysis of the returning waveform present on the input pin to the demodulator it was found that the main inhibiting factor was voltage ripple present on the supply voltage lines of the device as shown in figure 5.11. Although this noise was of very small magnitude (in the region of 5 to 10 mV), during filtering and amplification of the tag backscatter this noise was being amplified to a substantial level and hindering the reception of the tag data.

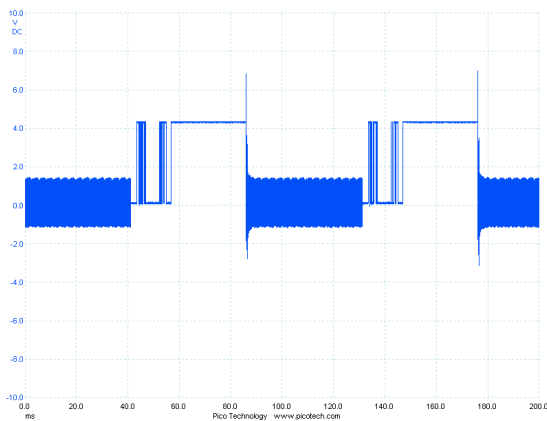


Figure 5.10: Bit-stream Resulting from Tag at 70cm

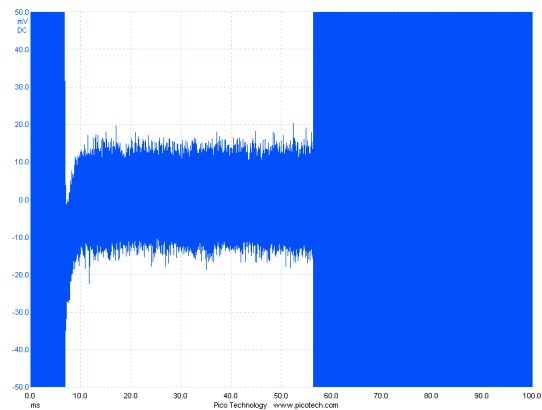


Figure 5.11: Noise Present on Device Power Supply Lines

5.7 Conclusion

This chapter has described the development of a low-cost animal Auto-ID reader module for use in the Dairymaster[®] milking parlour automation system. As can be seen from the Bill of Materials presented in Appendix A.6, the resulting animal Auto-ID module can be manufactured for a cost of under €30, compared with a cost of €249.59 for the Texas Instrument[®] module[14]. This will allow increased use of Auto-ID system for parlour automation, animal health monitoring and animal treatability with a

lower financial burden.

The reader module successfully generates a sufficiently strong EM activation field at a frequency of 134.2 kHz for the activation of HDX animal Auto-ID tags. Once activation has ceased, this reader module enters HDX listening mode and has the ability to receive and demodulate the FSK signal from any HDX tags present in the interrogation zone. During the HDX listening period the reader automatically retunes the antenna circuit to a resonant frequency of 130 kHz for the efficient reception of the FSK modulated HDX tag signal.

5.8 References

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Chapter 6

Case Study 3: DSP Based EMI Analysis and Animal Auto-ID System

6.1 Introduction

In recent years, companies that supply the agricultural sector with RFID technology have been encountering more and more problems with their Auto-ID systems as a result of areas becoming more hostile RF environments. The ISO standard requires animal Auto-ID systems to operate at 134.2 kHz, in the Low-Frequency (LF) license-free ISM (industrial, scientific, and medical) channel. RFID readers in the LF band are prone to Electromagnetic Interference (EMI) from electric motors, power invertors, high frequency lighting, cordless telephones, wireless headsets, wireless data networks, radio communications and other co-located readers which also operate in the LF ISM band. Each of these has the potential to introduce distortion products to the Auto-ID tag signal which may cause interrogation errors within the RFID system. This is a major problem with regard to milking parlour automation, which relies on the accurate identification of all animals within the parlour.

This chapter presents the development of a low cost system to analyse EMI within a milking parlour environment. The project concentrates on the investigation of EMI occurring in the frequency spectrum close to 134.2 kHz which greatly affects the operation of ISO standardised animal Auto-ID RFID systems. The intention is to provide a technician or engineer with a user-friendly system to observe and identify EMI in a dairy farm environment. This will allow the technician to make informed decisions with regard to system installation and allow the characterisation of EMI within a dairy environment.

The characterisation of EMI within the dairy environment has led to the development of a prototype system which demonstrates the potential for the use of DSP in the area of EMI resistant HDX animal Auto-ID readers in the later part of this

case study. The operation of these HDX Auto-ID systems has been described in detail in Chapter 3. In this case study a system will be developed to operate effectively in the presence of strong EMI outside of the 120 – 140 kHz frequency band. EMI within this band will be dealt in a later case study. This prototype will only deal with the reception and demodulation of the tag's response.

6.2 A Low-Cost Low-Frequency EMI Analysis Tool

6.2.1 Objectives

This section of the case study aimed to develop a low cost system with the ability to receive and analyse EMI found within a dairy environment. This will allow investigation of EMI occurring in the frequency spectrum close to 134.2 kHz which greatly affects the operation of ISO standardised animal Auto-ID systems. The intention was to provide a technician or engineer with an affordable solution for the identification of LF EMI which may affect overall parlour automation. Based on initial testing with a Dairymaster[®] animal Auto-ID system, it was found that EMI occurring within the band 100 kHz to 160 kHz has a severe effect on the operation of the system, therefore the system developed here will focus on this frequency band.

Currently, Dairymaster[®] use a voltage level taken directly from their animal Auto-ID RFID system as a measure of the amount of EMI present in a milking parlour installation. This voltage level represents the EMI detected by the Auto-ID system antenna. At the point where this voltage is taken, the EMI has been received, filtered and amplified by the RFID system and is about to be presented to the RFID systems signal demodulation stage. While this method proves effective in identifying the presence of EMI, it gives almost no information of the frequency, magnitude or spectral composition of the EMI.

To aid the elimination of EMI in an agricultural setting it is vital to be able to make a detailed analysis of the EMI present. Such an analysis should yield information including the spectral components and corresponding magnitudes of the EMI. Armed with this information, it is often easy to quickly identify the EMI source

and deal with the issue. A detailed knowledge of the composition of the EMI present in an agricultural setting is also needed if future Auto-ID systems are to be designed which can automatically account for these interferers and operate as designed.

6.2.2 Electro-Magnetic Interference

EMI often referred to as “noise“, is any unwanted externally generated signal which enters the signal path of a device [1]. Such unwanted signals can often be separated into two distinct groups based on the method by which they enter the signal path of interest; ‘conducted’ and ‘radiated’. Conducted EMI will enter the system through some physical electrical connection, while radiated EMI is coupled into the circuit through capacitive or inductive coupling between the device components and the EMI source. Such noise sources include electric motors, power invertors, RF communication transmissions and lighting systems. [2]

This case study will deal specifically with the analysis of radiated EMI which greatly affects the operation of wireless RF systems. While conducted EMI can often be accounted for and removed through effective filtering methods on the power stage, radiated EMI is received through the antenna stage of an RF receiver. If this EMI is occurring at or near the frequency at which the RF system is operating it becomes extremely difficult to filter from the system.

EMI is often classified into two main categories; random, often described as ‘bursty’ and deterministic, often referred to ‘continuous’ or ‘narrowband’. Bursty EMI takes the form of a random electromagnetic (EM) interferer signal, often localised in nature. For a system to broadcast over a wide bandwidth, increased power is required. Therefore, bursty EMI sources often emit EMI as a byproduct of some other operation, often due to a system malfunction. These emissions are often of low power as higher power emissions would make the system highly inefficient at performing its intended purpose. The lower power of these emissions result in bursty interference issues often being localised in nature. Sources of localised bursty EMI include electric motor, power inverters, automotive ignition systems and lighting systems. Deterministic interferer signals are intentionally created narrowband EM signals, often with fixed transmission frequency and amplitude. These signals are often emitted by communication systems and high-voltage power lines. By the nature

of their operation, these EMI signals may have an interfering effect on equipment located large distances from the source. [3]

6.2.3 EMI Analysis System Requirements

The analysis of EMI in the LF band in an agricultural environment requires a portable system for the reception, storage, processing and display of the EM signals present. Such a system would include a LF antenna system, a data acquisition system and a storage, processing and display unit. The display unit should have the ability to present the data in an easily readable and interpretable fashion. The storage unit should have the ability to store large volumes of data, in the order of many megabytes(MB). The unit should also have the ability to convert the received EMI signals to a short-term frequency-domain spectrum covering the LF band and display this spectrum in real-time. It is also required that the system can be supplied to technicians and engineers at a low cost, to allow widespread adoption of the system within industry.

6.2.4 Existing EMI Analysis Systems

Specialised EMI receivers are designed for the reception and analysis of EMI signals. Initial investigations showed that specialised EMI receivers used for the analysis of EMI were outside the budgetary constraints of this project. Many of these receivers operate in much the same way as lower-cost and more commonly available spectrum analysers [4]. Therefore it was decided to focus on the spectrum analyser method of EMI analysis. Consultations were made with a number of company representatives specializing in the analysis of real-world EMI signals. These representatives recommended the use of a portable spectrum analyser in conjunction with an antenna system tuned to the LF band.

A spectrum analyser is a device used to examine the spectral composition of a signal presented to it. These devices operate by decomposing the signal into its frequency components and measuring the amplitude associate with each component. This is often performed by applying a Fourier transform (or an equivalent operation) to the input signal. This has the effect of transforming the signal from the time-domain to the frequency domain. The result is then displayed in an amplitude versus frequency plot. With the increased computing power available to many modern digital

oscilloscopes, many are now able to perform the Fourier transform on a signal, hence making them a low-cost alternative to the spectrum analyser.



Figure 6.1: Rhode&Schwarz[®] FSH4/8



Figure 6.2: Tektronix[®] SA2600

In order to evaluate the use of a spectrum analyser for the purpose of on-farm EMI analysis, two different units, the Rhode&Schwarz[®] FSH4/8 Handheld Spectrum Analyser [5], shown in figure 7.1, and the Tektronix[®] SA2600 Spectrum Analyser [6], shown in figure 7.1, were acquired for a short period from their respective distributors in Ireland. The Rohde&Schwarz[®] device was also supplied with a low-frequency antenna system, the Rohde & Schwarz[®] HE300HF Active Directional Antenna [7].



Figure 6.3: PicoScope[®] 3424

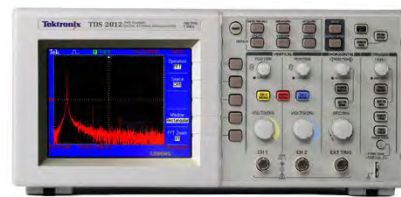


Figure 6.4: Tektronics[®] TDS2002

Two other ‘lower-end’ devices, the PicoScope[®] 3424 [8], shown in figure 7.3 and the Tektronix[®] TDS2002 [9], shown in figure 7.4, which have the ability to operate as a spectrum analyser by performing the Fourier transform on a received signal, were also tested. The PicoScope[®] 3424 is a 10 MHz PC oscilloscope with 12-bit sample resolution and an internal memory of 128 MB. It can be connected to a PC via USB interface, which allows the data acquired by the device to be displayed using the supplied PicoScope[®] 6 software [10]. This software has a spectrum function which

computes and displays the Fourier transform of the signal received allowing the efficient identification of the EMI amplitude and frequency. The Tektronix® TDS2002 [9] is a standard digital desktop oscilloscope with an option of displaying the Fourier Transform of a signal through the use of its ‘Math function’.

6.2.5 Low-Frequency Antenna Systems

As this case study focuses on the analysis of EMI which may affect the operation of an animal Auto-ID RFID system, an antenna circuit similar to those used in these Auto-ID systems was designed for use in this EMI capture system. LF RFID systems use a resonant Resistive-Inductive-Capacitive (RLC) antenna circuit system for the reception of electromagnetic signals. This circuit takes the form of a loop antenna (inductor) and a tuning capacitor. The components of the antenna circuit are chosen to allow the antenna circuit to be resonant at the operating frequency of the RFID system (134.2 kHz) according to equation 6.1.

$$f_R = \frac{1}{2\pi\sqrt{LC}} \quad (6.1)$$

A similar antenna circuit was designed for the purpose of receiving EMI signals using the Texas Instruments® Series 2000 RI-ANT-G01E loop antenna [11]. This antenna consists of a loop of wire creating an inductance of 27 μ H. Applying equation 6.1, a capacitance of approximately 52 nF, placed in parallel with the antenna loop, is required to tune this antenna circuit to resonate at 134.2 kHz. A resistor is also placed in parallel with the loop and capacitor to act as a resonance damper, resulting in a flatter, broader magnitude-frequency response to the antenna circuit. This allows the antenna circuit to accurately receive EMI occurring over the range 120 kHz to 160 kHz, but giving a slightly greater emphasis to those signals occurring closer to the operating frequency of the RFID system. A diagram of the antenna circuit is shown in figure 6.5.

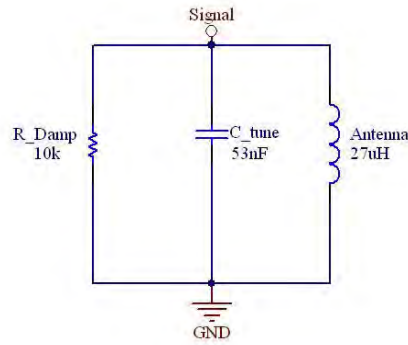


Figure 6.5: Resonant Antenna Circuit

The Rohde&Schwarz[®] distributor in Ireland also supplied this study with the HE300 Active Directional Antenna System [7]. This antenna system is described as “portable directional antenna for tracing signal transmitters and interference sources”. It is claimed that the direction of the signal source can be found by pointing the antenna towards the direction of maximum signal voltage. For this antenna system to operate in the LF band, the optional HE300HF antenna fitting was also provided. This fitting has a frequency range spanning from 9 kHz to 20 MHz.



Figure 6.6: HE300HF Directional LF Antenna

6.2.6 System Testing

Low-Frequency Antenna System Testing

Both antenna systems were tested with the Rhode&Schwarz[®] FSH4/8 Handheld Spectrum Analyzer. It was found that, due to the HE300s built in pre-amplification stage, that the EMI signal received by this antenna was of much greater amplitude. This unfortunately did not increase the clarity of the EMI signal of interest as all base-band EMI was also amplified by the pre-amplifier. It was also found that, while the

HE300HF had a much greater bandwidth (9 kHz to 20 MHz), the resonant antenna circuit performed equally well in the frequency band of interest (120 – 160 kHz).

Testing also showed the direction finding capability of the HE300 antenna system proved to be largely based on a ‘trial and error’ method during which the EMI signal amplitude will vary with respect to various antenna locations and orientations. It was found that the direction finding capabilities on resonant antenna circuit compared very favourably with that of the HE300 system.

Having found that both antenna systems performed the required task to a very similar level, the decision of which antenna system to use for this EMI analysis system was based upon the financial cost associated with each antenna system. The HE300 Active Directional Antenna System is priced at \$8130 (€5,500.24), \$6430 (€4,350.13) for the antenna set plus \$1700 (€1,150.11) for LF antenna option [12] while the purpose-built LC resonant antenna circuit cost a total of €154.43 (Antenna Loop €154.28 [13], Capacitors: €0.10 Resistor €0.05 [14]). This makes the purpose built RLC resonant antenna circuit the obvious choice for use in this system.

The cost of this antenna circuit can be further reduced by producing a loop antenna ‘in-house’ to replace the Texas Instruments® Series 2000 RI-ANT-G01E loop antenna, which is composed of a 27 uH loop of high-quality wire.

Spectrum Analyser Testing

Initial evaluation of the spectrum analysers took place in a laboratory setting, with various EMI sources, such as waveform generators and unfiltered power invertors, present. Each spectrum analyser tool (together with an LF antenna) was tested to determine if it could successfully detect the correct frequency of the EMI source in use and also if the source could be located by observing the change in the signal amplitude as the location of the antenna changed.

Upon testing of each of the systems mentioned above, it was found that all four had the ability to detect strong EMI signals in real-time. The spectral composition of these signals could be viewed immediately on the display and by moving and rotating

the LF antenna a good estimation of the location of the EMI source could be determined.

In the presence of weaker EMI signals it was found that the Tektronics® TDS2002 Oscilloscope performed poorly. This was mainly attributed to the fact that the display on the unit is quite small and the magnification function available did little to enable accurate frequency and magnitude analysis. The TDS2002B is priced at €1160 representing a very economic option to industry [9].

Both the Tektronix® H600/SA2600 Spectrum Analyzer and the Rhode&Schwarz® FSH4/8 Handheld Spectrum Analyzer performed well, detecting the EMI present in the LF band with a high degree of accuracy and easily magnified displays. Both had the ability to identify the frequency of the presented EMI and, by moving the antenna, the EMI source could be located by ‘trial and error’, based on the EMI signal amplitude with respect to various antenna locations and orientations. Both of these options prove highly expensive, with the Tektronics® SA2600 priced at €21000 [6] and the Rohde&Schwarz® spectrum analyser priced at \$9220 [12].

The PicoScope® 3424 proved to be the device most suited to this application. While the PicoScope® itself has a degree of on-board processing power, it is its ability to access the processing and data storage capabilities of a PC (or laptop) that allows it to perform to a similar level to that of much higher-end devices. The supplied PicoScope® software, which operates on the PC, has a very accurate ‘Spectrum’ function which produces a very high resolution Fourier transform of the received signal with a resolution similar to that of the Rohde&Schwarz® and Tektronics® purpose-built spectrum analysers. It also proved far more user friendly than the other devices tested, as the user-interface of this device is based on a Windows® based system allowing technicians with moderate PC skills to be quickly trained to operate this device. This device also represents a very economical solution at a cost of €873.75. [8]

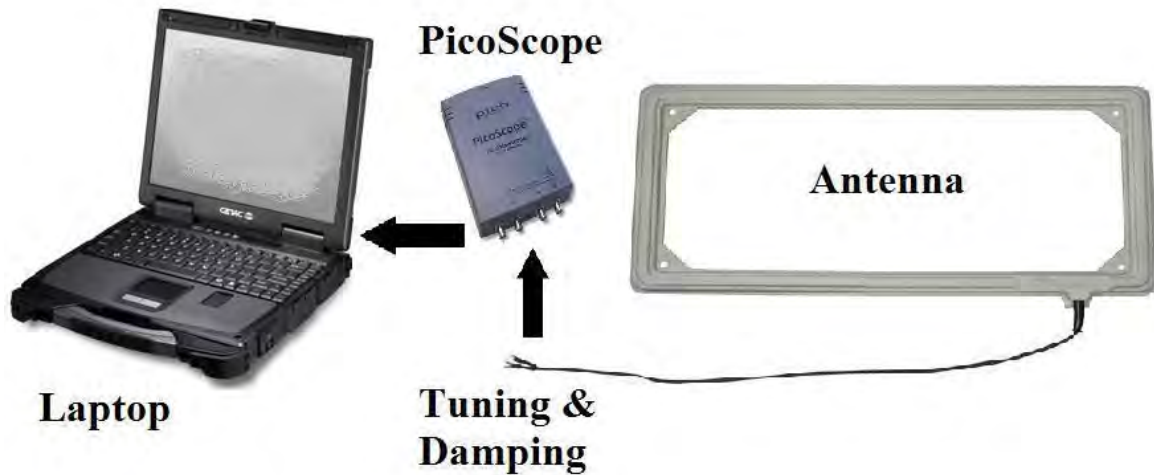


Figure 6.7: Complete EMI Analysis System Used in this Study

6.2.7 Site Survey: On-Farm EMI Analysis

To evaluate the effectiveness of the developed system, comprising of the PicoScope[®] 3424, a laptop computer and a LF resonant antenna circuit, it was tested on a number of farms which were suggested by Dr. Edmond Harty and Mr. John Collins of Dairymaster[®]. Two farms in Ireland were selected along with two farms in Germany. Three of these four farms have a history of EMI curtailing the operation of an animal Auto-ID system. The remaining farm has a history of extremely low EMI levels resulting in excellent animal Auto-ID read-rates.

Site Survey 1: Dairy Farm Facility at Causeway, Co. Kerry Ireland

This farm was chosen for a site survey as it has a history of excellent animal Auto-ID system operation, generally operating at a read-rate of 100% i.e. zero animal Auto-ID tags are missed in a given milking. This would lead one to believe that the farm, in conjunction with having well installed and suitably located Auto-ID system antennas, has a very low level of EMI within the frequency band of the Auto-ID system. Therefore, the results of the EMI analysis made at this site can be used as a base-band for future site surveys. The frequency spectrum of the EMI present and received by the EMI analysis system is shown in figure 6.8. As can be seen from this figure, the EMI signal level received by the EMI analysis system never rises above approximately -110 dBu in the band 120 kHz to 140 kHz.

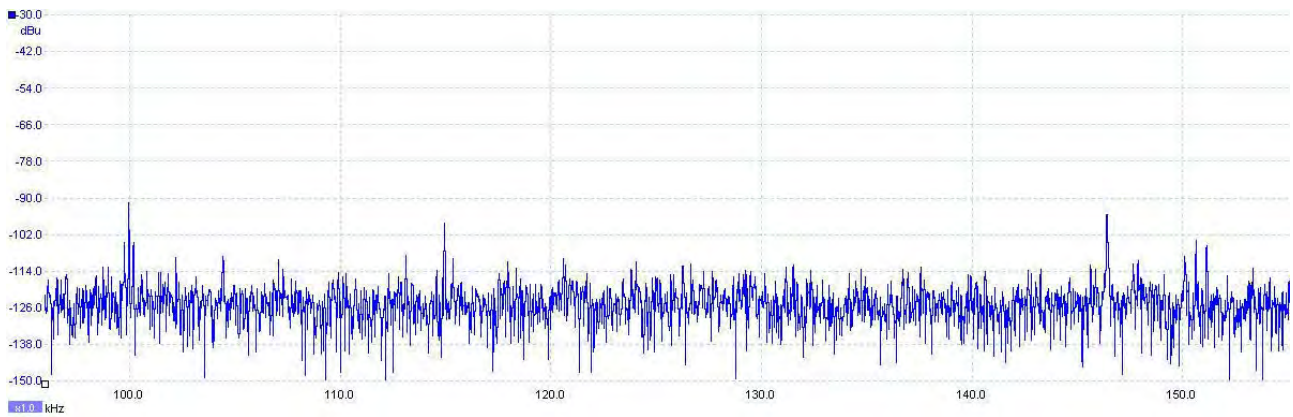


Figure 6.8: Spectrum of EMI Received at Survey Site 1

Site Survey 2: Dairy Farm Facility at Ballingarry, Co. Limerick

This farm was chosen as the second site survey to be carried out as it has on-going EMI issues with regard to the installed animal Auto-ID system. Dairymaster[®] engineers had already tracked the source of the EMI to a high-frequency fluorescent lighting installation approximately 150 m from the Auto-ID enabled drafting gates. The lighting system was identified by process of elimination involving the successive deactivating of any potential noise source until the Auto-ID system functioned correctly.

Figure 6.9 presents the spectrum analysis taken when the high-frequency lighting close to the Auto-ID enabled drafting gate is de-activated. Some peaks can be seen, but the band of 120 kHz to 140 kHz has a very low EMI level. Figure 6.10 presents the frequency spectrum obtained with the lighting activated. A clear ‘hump’ can be seen between approximately 135 kHz to 140 kHz with EMI levels rising to greater than -90 dBu, along with a slight rise along the entire frequency spectrum. This introduction of EMI has a detrimental effect on the operation of the facilities animal Auto-ID system.

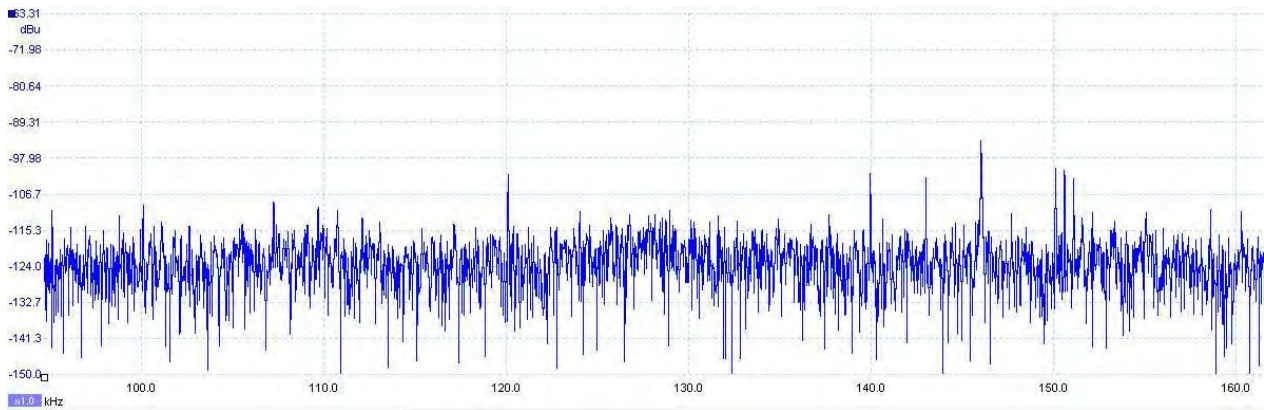


Figure 6.9: Spectrum of EMI Received at Survey Site 2 with Lights Off

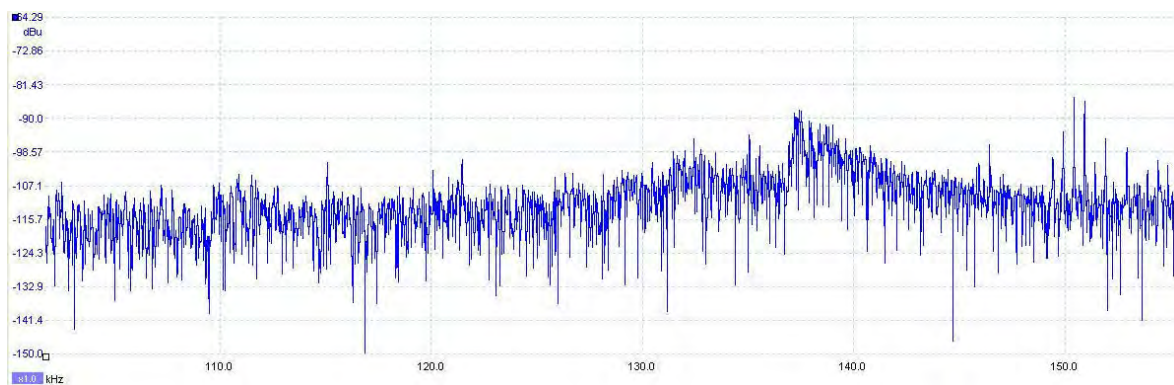


Figure 6.10: Spectrum of EMI Received at Survey Site 2 with Lights On

Site Survey 3: Dairy Farm Facility at Neuzenheim, Iphofen Germany

In central and Eastern Europe there is a concentration of high-power LF transmitters used for the purposes of time-signal transmission, power-load regulation and emergency communications. Such transmitters include DCF-39, DCF-49, and DCF-60, which operate at the frequencies of 139 kHz, 129 kHz and 140 kHz respectively [15]. The transmitters DCF-49 and DCF-60 are located at Mainflingen, just outside Frankfurt. DCF-39 is located in Madgeburg, Germany.

A spectrum analysis of the EMI taken at the farm in Neuzenheim, Germany is shown in figure 6.11. Neuzenheim lies approximately 80 miles east of Frankfurt and 150 miles south-south-west of Madgeburg. From the frequency spectrum shown in figure 6.11, peaks at the frequencies 139 kHz, 129 kHz and 140 kHz can be clearly seen. This would indicate that these transmitters are the cause of the EMI which has caused problems with the farm's animal Auto-ID system. An additional unidentified peak at 120 kHz is also clear in the spectrum.

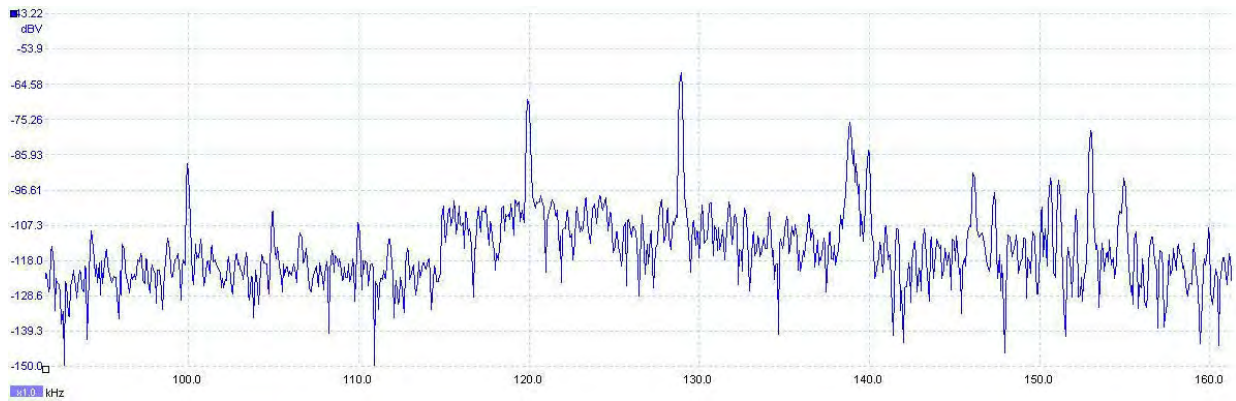


Figure 6.11: Spectrum of EMI Received at Survey Site 3

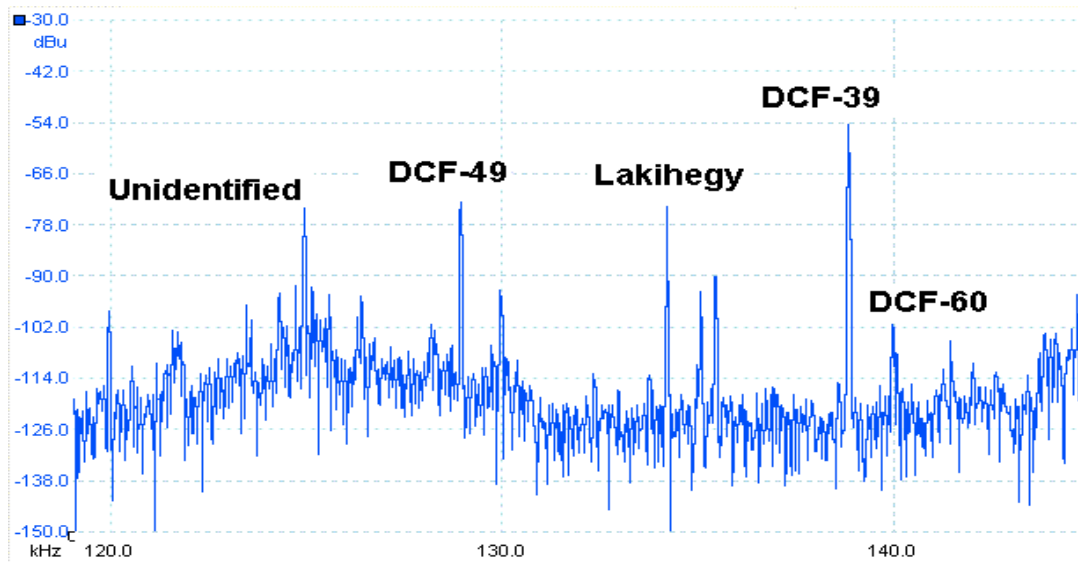


Figure 6.12: Spectrum of EMI Received at Survey Site 4 with Data Transmitters Labelled

Site Survey 4: Dairy Farm Facility at Gorzke, Germany

The farm located in Gorzke, Germany (approximately 60 miles South-West of Berlin) is also affected by EMI which is caused by the data transmitter systems which are prominent in Central Europe. This farm lies approximately 30 miles to the east of Madgeburg and approximately 250 mile north-east of Mainflingen, the transmission sites of the EMI signals detected on the Neuzenheim farm.

Figure 6.12 shows the frequency spectrum of the EMI received at this location. Many of the peaks in this spectrum have been labelled with the name of the

transmitter which is responsible for that peak. An additional transmitter operating from Lakihegy, just south of Budapest and approximately 400 miles from Gorzke, was also identified as the transmitter operating at 135.6 kHz.

6.2.8 Results and Discussion

A portable low-cost EMI analysis tool has been developed. The system has the ability to receive, digitise, store and present the LF EMI present in a dairy facility. The system has been tested and evaluated ‘on-site’ and performs as described, with the ability to identify the amplitude and frequency of LF EMI present on site. This has in turn led, in many instances, to the identification of the EMIs source both on and off farm.

During examination of the received EMI signals, it was noted that LF EMI can be broadly divided into two main categories; ‘bursty’ type Gaussian noise and ‘continuous’ interferer signals. Bursty type EMI signal are characterised as signals of varying amplitude and frequency, often centred on some mean with a roughly Gaussian distribution. They are often intermittent and, due to the wide-bandwidth nature of their transmission, localised. The source of ‘bursty’ EMI can often be found on, or close to, the farm facility.

‘Continuous’ type EMI is characterised by a narrowband signal of constant frequency and amplitude, often emanating from an RF transmitter. The sources of this EMI type may be found at great distances from the farm, as the narrow-band nature of these signals makes efficient generation of high amplitude signals possible. This can often result in great difficulty in locating the exact source of this EMI and making elimination of the EMI impossible in many instances.

6.3 A DSP-Based Animal Auto-ID Reader

6.3.1 Objectives

This main aim of this section of the case study was to demonstrate that DSP is a suitable tool for use within an animal Auto-ID system. Section 6.2 has shown the harsh EMI environment often encountered in a dairy farm setting. This case study hopes to prove that through the use of DSP techniques, EMI can be filtered from the Auto-ID signal, resulting in a more reliable Auto-ID system. A DSP-based Auto-ID system was developed, utilising an extremely powerful band-pass filter which remove all EMI outside of the animal Auto-ID tags frequency band of operation.

6.3.2 Why Use DSP for Auto-ID?

In the area of Auto-ID technology, a DSP based system has a number of benefits over existing analogue based systems, specifically when the system must operate in the presence of EMI. Animal Auto-ID systems corresponding with ISO standards 11784 & 11785 [16, 17] operate in the frequency band of 120 – 140 kHz. To successfully demodulate a response from a HDX animal Auto-ID tag, it is required that any EMI signal occurring outside of this frequency band is removed. This requires a band-pass filter with a steep roll-off gradient, a centre frequency of 130 kHz and a bandwidth of 20 kHz.

The analogue band-pass filters, used to remove interfering signals which occur outside of the frequency band in use, become extremely large and complex when steep roll-off gradients are required. While still large and complex, DSP based band-pass filters can be developed and implemented more easily and cost-effectively using development platforms such as the MATLAB[®] [18] prototyping environment. With the advent of cheap re-configurable ICs such as CPLDs (Complex Programmable Logic Device) and FPGAs (Field Programmable Gate Array) which contain many millions of user programmable logic gates, the realisation of such large digital filters can be achieved at a low cost in a relatively short time-scale.

In addition, if an interferer signal occurs within the frequency band of interest, it may be impossible to remove it using conventional filtering methods without also

removing what may potentially be a signal from an Auto-ID tag. In such situations an intelligent DSP based system must be implemented which can differentiate between EMI and a tag response signal. Such techniques would involve the characterisation of interference signals during the absence of Auto-ID tags, hence allowing additional signals outside of this characterisation to be identified as tag signals.

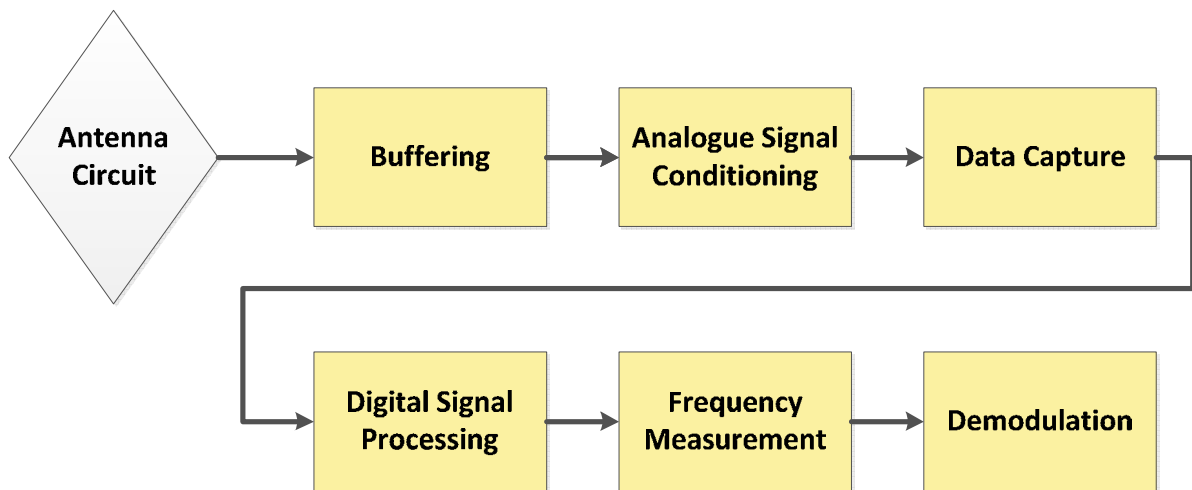


Figure 6.13: Block Diagram of DSP Animal Auto-ID Reader Prototype

6.3.3 System Overview

Figure 6.13 presents a flow diagram of the prototype Data Capture, Data Digitisation and DSP system developed during this case study. Firstly the response of an activated HDX animal Auto-ID tag is received by a tuned antenna circuit. The analogue output of this antenna circuit is then buffered and high-pass filtered to remove the DC component. The signal is then captured and digitised using an appropriate PC-based data capture device and imported into the MATLAB[®] prototyping environment for DSP filtering, frequency measurement and demodulation.

6.3.4 Signal Capture

In order to apply DSP techniques to the reading of animal Auto-ID tags, a data acquisition system must be developed which can successfully receive the response from an animal Auto-ID tag. This analogue signal response must then be digitised and subsequently imported into a DSP environment.

Firstly a tuned resonant antenna circuit is required to receive the response from an activated HDX Auto-ID tag. This consists of a loop antenna of inductance $27\mu\text{H}$ and a capacitor of suitable values that allow the circuit to resonate at 130 kHz. Equations 6.2 and 6.3 can be used to choose the correct capacitance values to tune the antenna circuit to resonance. The tuning of such an antenna circuit is described in detail in Case Study 1.

$$f_R = \frac{1}{2\pi\sqrt{LC}} \quad (6.2)$$

$$C = \frac{1}{4\pi^2 f_R^2 L} \quad (6.3)$$

It should be noted that the tag response signals to be received by this system originate from tags which have been activated by a 134.2 kHz activation field generated by a separate antenna powered by the circuitry described in Chapter 5.5.3.

A simple voltage limiter circuit is implemented at the output of the antenna circuit using two high voltage diodes as shown in figure 6.14. The output of the voltage limiter is then buffered using a standard Operational Amplifier (Op-Amp) based voltage follower buffer. This provides a high impedance connection for the antenna, hence reducing the effect of the signal capture circuit (especially the RC filter) on the operation of the antenna circuit. As the frequency band of interest (120 – 140 kHz) is relatively high in terms of op-Amp operation, a current-feedback op-amp was used to create the voltage follower buffer. Current-feedback op-amps have a higher gain bandwidth product (GBW) than the more common voltage-feedback variety due to a reduced internal capacitance of the op-amp. This allows current-feedback op-amps to operate at higher frequencies. The op-amp chosen was the National Semiconductor[®] LM6181 [20] with a GBW of 100 MHz.

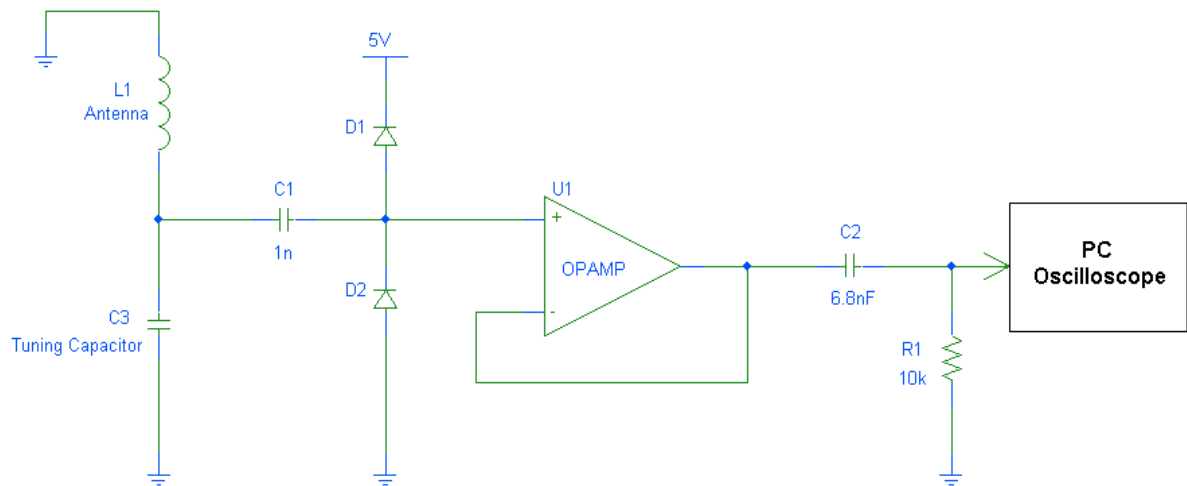


Figure 6.14: Low Frequency Data Acquisition System

An RC high-pass filter was placed just before the PC oscilloscope signal capture stage to remove the DC and extremely low frequency components of the waveform present on the antenna circuit. This allows the digitisation section of the data acquisition system to operate in its lowest voltage range setting, hence allowing the greatest possible voltage resolution. A low cut-off frequency of approximately 2000 Hz was required. The filter design formula is shown in equation 6.4.

$$f_{CUTOFF} = \frac{1}{2\pi RC} = \frac{1}{2\pi \times 10000 \Omega \times 6.8nF} = 2340 \text{ Hz} \quad (6.4)$$

The Picoscope[®] 3424 PC-based oscilloscope will be used as the data capture and digitisation tool for this system. ISO standards 11784 and 11785 [16, 17] detail that an animal tag must transfer all unique animal identifier information (along with header and CRC check) within a period of 20 ms after the suspension of the activation field. Therefore the PicoScope[®] 3424 was configured to capture the signal present on the antenna circuit for a total of 20 ms at a sampling rate of 10.4 MHz. This was made possible using the external trigger function of the oscilloscope which was connected to the control signal of the activation signal generator. Once the activation signal was deactivated the oscilloscope began data acquisition. As it was found during preliminary testing that the voltage range of the signal received from the animal tag

was never greater than 60 mVp-p, the input range of the PicoScope® was set to its lowest setting of 200 mVp-p.

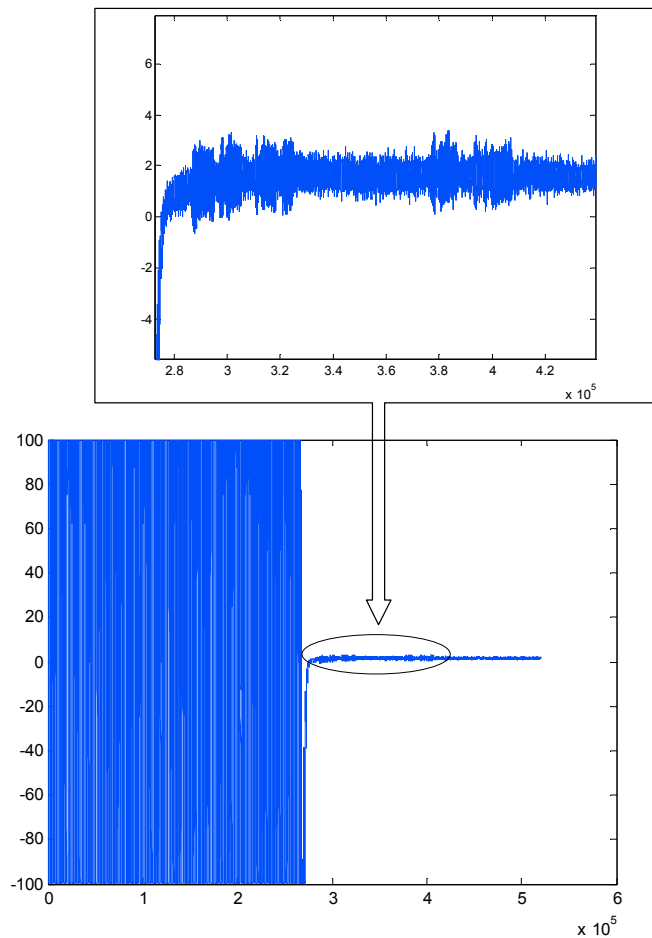


Figure 6.15: Data Capture of Noisy Auto-ID Tag Response Signal

At a 12-bit resolution, this resulted in a voltage resolution of 48.8 μV . Using the PicoScope® 6 software, the data acquired was then manually saved to a Comma Separated Variable (.CSV) file which contained a series of 208000 samples, each stored with a corresponding timestamp. A representative sample of the data captured by this data acquisition system is shown in figure 6.15. For demonstration purposes this sample was taken for 60 ms, with approximately the first 28 ms of the sample representing the reception of the Auto-ID activation signal.

6.3.5 Digital Signal Processing using MATLAB®

For this prototype the MATLAB® (MATrix LABORatory) prototyping environment for Windows® developed by MathWorks Inc. [18] was used. MATLAB® is an interactive technical computing environment and programming language which

specialises in the areas of algorithm development, data analysis and numeric computation. A large number of MATLAB[®] add-on products are available which contain user interfaces and functions for specialised technical areas. For the development of DSP algorithms the MATLAB[®] DSP processing toolbox was used. The data captured using the system described in section 6.3.4 can be easily imported into the MATLAB[®] prototyping environment for processing.

Investigation of Bandpass Filter Design Parameters

It is interesting to note that, while the Frequency Shift Key (FSK) modulation scheme for the response of these tags is designated to be 124.2 kHz for a logic ‘1’ and 134.2 kHz for a logic ‘0’, the true response of most animal Auto-ID tags is quite different. From the examination of the signal transmitted by many HDX animal Auto-ID tags upon activation, it was found that the frequency transmitted to represent a logic ‘1’ often varies between 120 kHz up to approximately 129 kHz, while a frequency varying between 130 kHz to 138 kHz can represent a logic ‘0’. The exact frequency used to represent a logic value regularly varied within the response from a single tag during a single read, as shown by a spectrum analysis of a single read from a sample tag in figure 6.16. It was found during experimentation, using a selection of 20 Texas Instruments[®] TIRIS Auto-ID tags [19], that all 20 tags tested behaved in this manner.

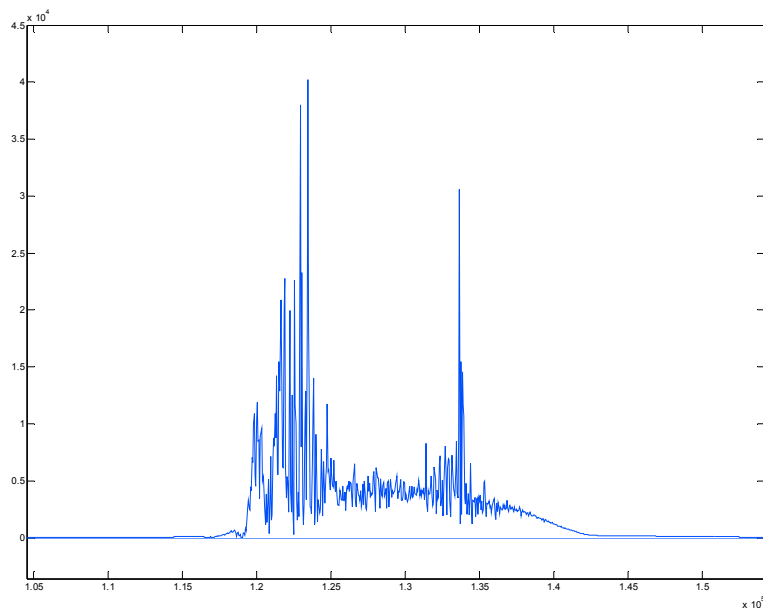


Figure 6.16: Spectrum Analysis of Tag Response

DSP Bandpass Filter

The tag signal data captured using the PicoScope[®] PC oscilloscope and PicoScope[®] 6 software was then imported to MATLAB[®] as a 208000 sample array. As shown in figure 6.16, a HDX animal Auto-ID tag responds within the frequency band 120 – 140 kHz, therefore any signal occurring outside of this band is of no use to the system and considered interference. To remove this interference, a 3000th order bandpass Hamming-window based, linear-phase Finite Impulse Response (FIR) filter with a centre frequency of 130 kHz and a bandwidth of 20 kHz was created within MATLAB[®]. This filter provided an extremely steep, almost vertical signal roll-off outside of the pass-band. An example of the resulting signal is shown in figure 6.17.

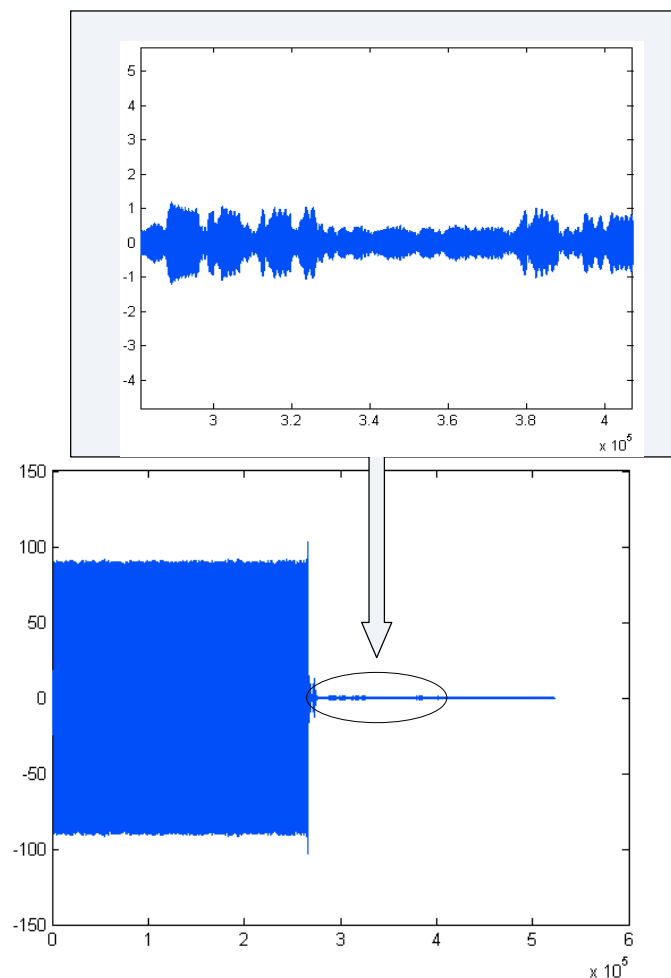


Figure 6.17: Filtered Tag Response

The mathematical representation of an FIR filter is shown in equation 6.5.

$$Y[n] = b_0 X[n] + b_1 X[n-1] + b_2 X[n-2] + \dots + b_{2999} X[n-2999] \quad (6.5)$$

where X is the discrete signal and b is the array of filter coefficients.

The filter coefficients array, b , was designed in MATLAB[®] using the Hamming-window FIR filter design method implemented by the MATLAB[®] filter design tool “FIR1”.

Discrete Signal Demodulation

Within MATLAB[®] an algorithm was developed to demodulate the FSK data modulation scheme of the ISO animal Auto-ID tags response. As described earlier this FSK modulation scheme takes the form of a 124.2 kHz signal for a logic ‘1’ and a 134.2 kHz signal for a logic ‘0’. The method devised here operates by measuring the instantaneous frequency of each individual cycle of the received signal and then demodulating according to the FSK modulation scheme.

Following the filtering stage described in the previous section, the DC component of the signal was almost entirely removed. Now, the frequency of each cycle can be measured by locating the corresponding zero-crossing points of the signal. Based on the number of samples between each zero-crossing, an estimation of the frequency can be made. Shown in figure 6.19 is a waveform sampled at 10.4 Mega Samples Per Second (MSPS) which has been passed through the FIR filter described above. As can be seen, a full cycle of the waveform has been measured at 85 samples using the zero-crossing points. Dividing the sampling frequency, 10.4 MHz, by the number of samples, 85, yields the frequency of each cycle, in this case 122.35 kHz.

Here the zero-crossing point of the waveform was taken as the sample directly after the transition of the discrete signal from a negative to a positive value. At this point it was noted that in later revisions of this algorithm, a lower sampling rate of the signal might be required due to the limitations of cost and portability of the embedded

system. In such a situation, it may become difficult to differentiate between frequencies of the modulation scheme and a more advanced method of calculating the zero-crossing point would be required.

As the signal generated by the animal Auto-ID tag and subsequently received by the tuned antenna circuit, is the product of systems in resonance, it must take the form of a sine wave. Close to the zero-crossing (node) of a sine-wave signal, the signal can be approximated as a straight line, as shown in figure 7.18. Here the amplitude of the two points on either side of the zero-crossing point can be used to determine a closer approximation of the zero-crossing point.

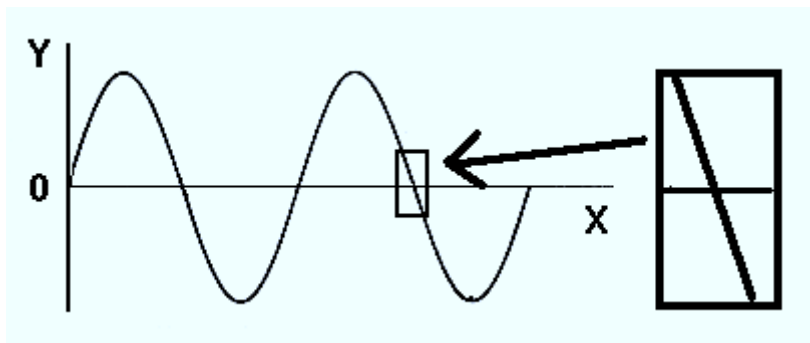


Figure 6.18: Sine-Wave with Magnification of Zero-Crossing Region

If we assume that both samples are close to the zero-crossing point, the standard equations of the line, given in equations 6.6 and 6.7, can be used to give an accurate estimation of the true zero-crossing point.

$$y - y_1 = M(x - x_1) \quad (6.6)$$

$$M = \frac{(y_2 - y_1)}{(x_2 - x_1)} \quad (6.7)$$

We now take A as the magnitude of the last negative sample point, X_1 , before a (negative to positive) zero-crossing and B as the magnitude of the next positive point, X_2 , after that particular zero-crossing. This gives two points on the line (X_1, A and X_2, B). If we allow X_1 to be a reference point and let it equal to zero we now have the points $0, A$ and X_2, B . Putting these into the equations 6.6 and 6.7 we get:

$$M = \frac{(B - A)}{(x_2)} \qquad y - A = \frac{(B - A)}{x_2}(x - 0)$$

At the zero-crossing point, y is equal to 0 and the equation becomes:

$$x = \frac{-Ax_2}{B - A}$$

and from this the location of the zero-crossing, with respect to the reference point of X_1 , point can be calculated

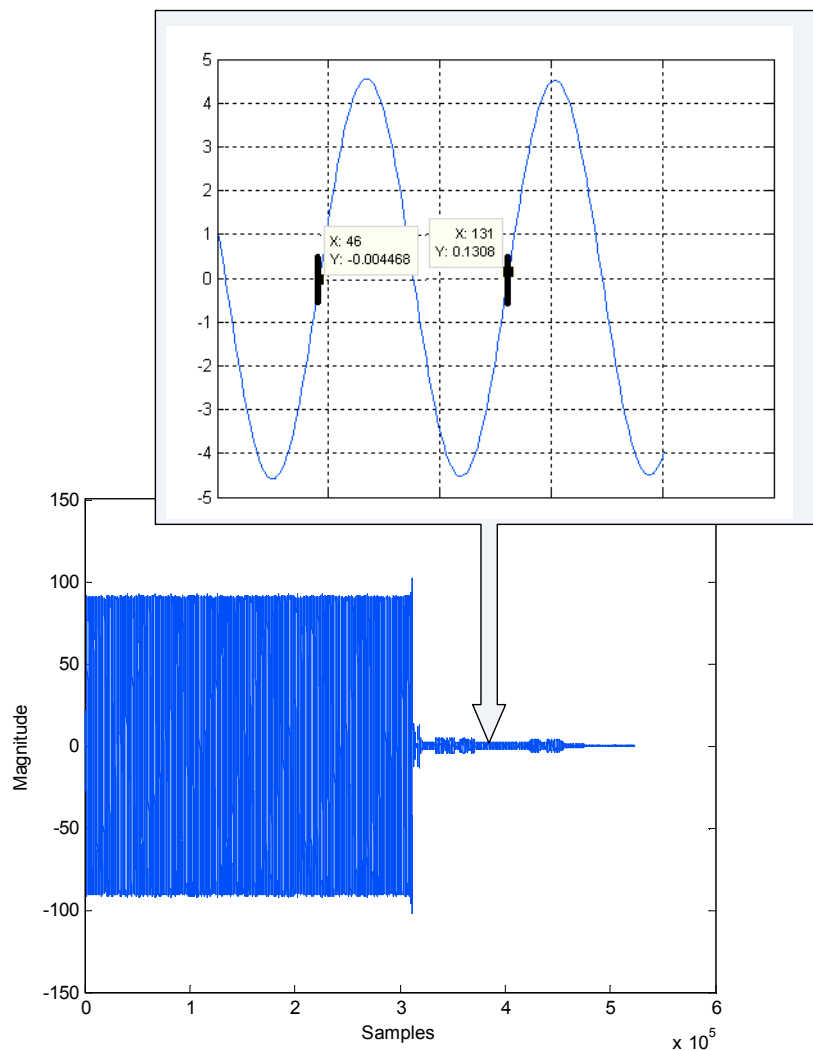


Figure 6.19: Zero-Crossing Measurement for Frequency Estimation

Once the frequency of each cycle of the discrete waveform is identified, a threshold of 129.2 kHz is applied and each cycle is listed as representing either logic '1' or '0'. Converting 129.2 kHz to a representative number of samples captured by the system operating at 10.4 MS/s we get a threshold of approximately 80.5. Applying this scheme, the cycle of the waveform analysed in figure 6.19 would be classified as representing logic '1'.

To complete demodulation, the array representing the logic value of each cycle is then analysed to detect sequences of 16 cycles of the same frequency, in accordance with the FSK demodulation scheme, where each bit is represented by either 16 cycles of 124.2 kHz or 134.2 kHz.

At this point it was found that if the demodulation scheme is strictly adhered to, the ID information is often incorrectly demodulated. It was found that better results were achieved if the array is firstly low-pass filtered with an averaging scheme to account for slight variations in the frequency of individual signal cycles.

6.3.6 Results

The resulting prototype HDX animal Auto-ID reader was tested using the experimental setup described in section 8.2.1, using the Dairymaster[®] calf feeder antenna for signal reception. In the presence of low-level EMI, the reader operated as designed and successfully receives and demodulates tag responses up to a range of approximately 25 cm to 30 cm. The resulting bit-stream was confirmed as correct by comparison with bit-streams received by the current Dairymaster[®] Auto-ID system and confirmed to be correct through the use of the CRC error detection algorithm.

When EMI outside of the frequency band 120 kHz to 140 kHz was introduced the reader operated as designed, with the FIR filter removing all signal components outside of the band of interest. It must be noted that any EMI present inside of the frequency band 120 kHz to 140 kHz could not be removed by the filter and therefore, when the EMI of significant magnitude was introduced within this frequency spectrum, the system failed to demodulate the tag response.

6.4 Discussion and Conclusions

This case study has presented the development of a portable low-cost system to effectively receive and analyse EMI within a milking parlour environment. The system is a highly economical and user friendly PC-based tool which will provide technicians and engineers with a method of ‘on-site’ EMI analysis at a relatively low cost with regard to both equipment and training. The system also allows the captured EMI to be exported as a data file from the PicoScope[®] 6 software. These data files can then be imported to an Arbitrary Waveform Generator (AWG), which, when coupled with an RF power-stage, matching network and antenna system, allows the recreation of the observed EMI in the laboratory.

The system has been tested and evaluated ‘on-site’ and performs as described. The final system is currently being used by Dairymaster[®] in the EMI analysis of current problem facilities and in the evaluation of potential system installation sites. It is envisaged that, as a direct result of this low-cost user-friendly EMI analysis tool, that a database of worldwide EMI samples can be created. Such a system would consist of a server or cloud based database in which users could upload EMI signal captures with an associated location. This would allow not only the examination of differing EMI characteristic worldwide, but also allow for a location-based EMI reference system which can be used by Auto-ID installation personnel, both in the planning and implementation phase.

On-site testing using the developed EMI analysis system brought to light the extreme conditions of the EM environment which are encountered within dairy farm facilities. This led to the requirement of a DSP-based Auto-ID system, which would allow advance EMI filtering techniques to be employed. This chapter has also presented the development of a prototype system which demonstrates the use of a DSP algorithm for filtering and demodulation of the response from animal Auto-ID tags. The system developed can successfully receive, digitise and import a tag response into a DSP environment. The algorithm developed within MATLAB[®] has been shown to successfully remove EMI from the signal and demodulated the tag signal using a FSK demodulation scheme.

This case study has shown that the application of Data Capture and DSP techniques to the field of animal Auto-ID readers has been successful and shows the potential for the use of further, more intelligent, DSP techniques in the field. This has led to continuing research in this area which is discussed in detail in Case Study 4.

During completion of this case study it was found that while MATLAB[®] has the ability to generate embedded code which can implement real-time algorithms, the MATLAB[®] prototyping environment is not well suited to real-time operation. For this reason the development of a real-time ‘stand-alone’ embedded system is proposed in Case Study 4.

6.5 References

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Chapter 7

Case study 4: An Advanced FPGA-Based Animal Auto-ID Reader

7.1 Introduction

The requirement for and benefits of a Digital Signal Processing (DSP) based animal Auto-ID reader has been outlined in Case Study 3. It has been shown that the application of Data Capture and DSP techniques can be successfully employed in animal Auto-ID readers, paving the way for the use of advanced DSP algorithms to aid tag interrogation in the presence of high level EMI. The previously developed DSP-based Auto-ID system operates within the MATLAB[®] prototyping environment [1], a platform which is not well suited to real-time operation. This greatly limited the testing of this device to single read tests in a laboratory setting.

For an advanced DSP-based animal Auto-ID system to be tested more thoroughly, a stand-alone real-time reader must be developed. Such an embedded system would require an independent DSP processing core, digital control, analogue signal conditioning and signal digitisation facility, together with an antenna circuit and activation signal generation power amplification stage.

This case study documents the development of a stand-alone DSP-based animal Auto-ID reader capable of real-time operation, which allows for more in-depth testing of the system and the development of novel advanced DSP-based algorithms to allow operation in high EMI environments. The system is based around a programmable logic device (PLD), which will allow the system to be reconfigured to account for variations in EMI within the environment in which the device is to operate.

7.2 System Requirements and Overview

To prove the concept of advanced DSP-based animal Auto-ID, the system developed here is required to be stand-alone device capable of real-time tag activation and signal reception, analogue signal conditioning, signal digitisation, DSP and animal Auto-ID signal demodulation. Its operation must conform to the timing schedule outlined in the ISO standardisation, as described in Chapter 3. While, this system focuses on the interrogation of Half Duplex (HDX) Auto-ID tags, hardware provisions are made for future development and reconfiguration of the system for Full Duplex (FDX) tag interrogation.

For such a system to be realised, all DSP must be performed within the embedded system, with the ability for high through-put of signal data and real-time signal demodulation capabilities. The system must also incorporate and control the antenna circuitry, analogue filtering and activation field generation electronics.

In recent times the development of high-speed, efficient and low-cost dedicated DSP integrated circuits (ICs) have provided suitable methods for the implementing embedded DSP algorithms, which can achieve real-time operation. As described in section 2.6.1, more recently, the Field Programmable Gate Array (FPGA) has been used in the implementation of DSP algorithms. Certain advantages have been found in the use of FPGAs over dedicated DSPs in the implementation of DSP algorithms. FPGAs are inherently parallel, meaning that many operations can be carried out in a single system clock cycle. The advantages of such a feature can be seen immediately in the implementation of repeated multiplication stages of a DSP algorithm.

This system is divided into two discrete hardware sections; firstly, the analogue and digital electronic hardware and secondly the digital hardware configuration within the FPGA. The initial prototype is designed as an add-on board to the Xilinx[®] Spartan 3e Development Board [2] and is used to verify the operation of the device control and data acquisition sections of the system. In the final prototype the digital hardware, including advanced DSP hardware, is configured on the

Xilinx® Spartan 3e FPGA mounted on Enterpoint® Darnaw1 Pin Grid Array (PGA) FPGA module [3].

7.3 Analogue and Digital Hardware

The analogue and digital hardware required for an advanced DSP-based Animal Auto-ID system can be divided into 5 sections. Firstly an FPGA is required to provide all digital control and DSP operations. A series of power supplies are required to power the various sections of the system, an antenna circuit and power amplification stage is required to form the RF interface between the system and the Auto-ID tag under interrogation. An analogue signal conditioning section is needed to prepare the signal for digitisation.

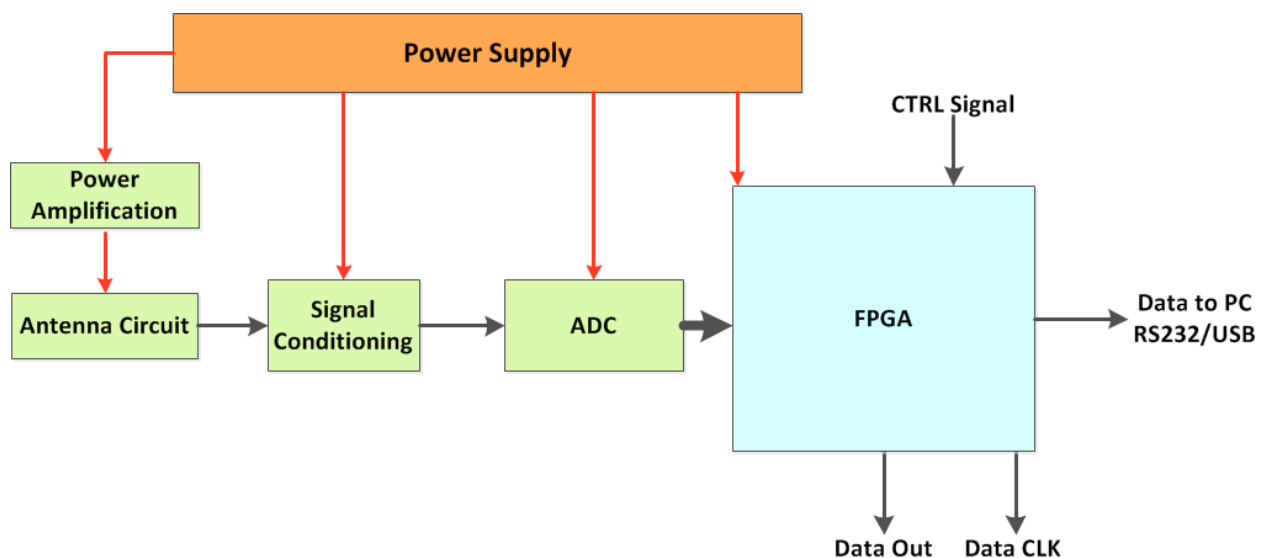


Figure 7.1: System Hardware Overview of FPGA Auto-ID System

Digitisation is performed by a high-speed precision Analogue-to-Digital Converter (ADC). All of these sections will now be described in greater detail. A block diagram of the system hardware can be seen in figure 7.1.

7.3.1 Field Programmable Gate Array (FPGA)

The FPGA to be used for this design is the Xilinx[®] Spartan 3e, as supplied on the Xilinx[®] Spartan 3e Starter Kit FPGA development board and the Enterpoint[®] Darnaw1, shown in figures 7.2 and 7.3 [2, 3].



Figure 7.2: Xilinx[®] Spartan 3e Starter Kit [2]

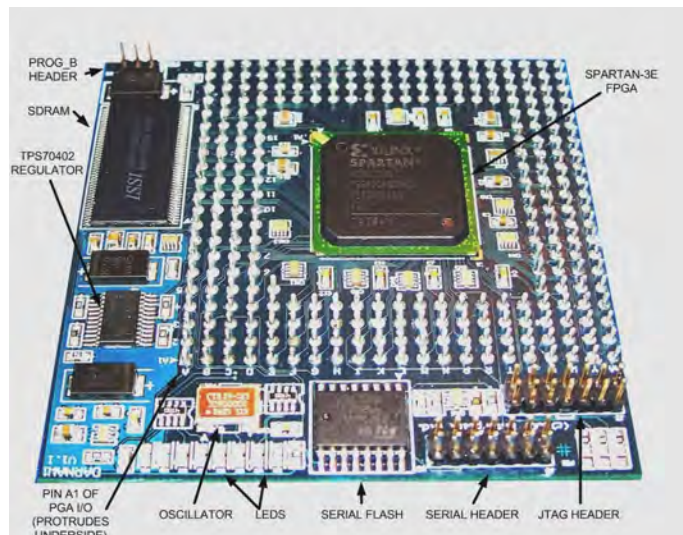


Figure 7.3: Enterpoint[®] Darnaw1 Spartan 3e FPGA Module [3]

The Xilinx® Spartan 3e Starter Kit is supplied with the Spartan 3e XC3S500E-4FG320C FPGA [4]. This device is used as a controller in the initial prototype to ensure correct operation of the external system hardware. Once this signal conditioning hardware was found to be functioning correctly, the Xilinx® Spartan 3e Starter Kit was replaced with the Enterpoint® Darnaw1 module. The Enterpoint® Darnaw1 is supplied with the Spartan 3e XC3S1600E-4FGG400C FPGA [4]. The key factors identified for the evaluation of FPGAs for this project were; Capacity, Operating Speed, Hardware Multiplier Units, Dedicated RAM, Digital Clock Managers and Unit Cost. These will now be discussed in greater detail with reference to the chosen FPGA.

Capacity

It is vital that the chosen FPGA has a sufficient number of available programmable logic gates for the implementation of the desired system configuration. Upon synthesis of the proposed design with the Xilinx® ISE development environment, a synthesis report is generated which contains documentation of the number of gates required within the target FPGA for the design to be implemented. This amount of gates required to implement a design is highly device specific as varying FPGA types have varying numbers of hardware multipliers, adders, Random Access Memory (RAM) blocks. The Xilinx® Spartan 3e (XC3S1600E-4FGG400C) has 1600,000 programmable logic gates.

Operating Speed

The Xilinx® ISE development environment has the ability to make a prediction of the maximum operating speed a device will achieve for a synthesised configuration. The chosen FPGA device will have to operate at a suitable clock speed to successfully accept and process sample data from the ADC at a rate of 10 MSPS.

The Xilinx® Spartan 3e (XC3S1600E-4FGG400C) has a Xilinx® speed grade of 4. When the realised VHDL design was synthesised with Xilinx® ISE, with the Xilinx® Spartan 3e (XC3S1600E-4FGG400C) set as the target device, it was shown that the configured device had the ability to operate at 21.7591 MHz

Hardware Multipliers

Certain FPGAs have dedicated hardware multipliers, which can be accessed directly by the FPGA configuration for miscellaneous multiplication operations. Some DSP specific FPGAs have dedicated hardware multipliers contained within dedicated DSP 'slices'. These slices often contain addition adders and registers to facilitate hardware, single clock cycle, multiply accumulate operations (MACs). Such a device is the Xilinx[®] Virtex 7 FPGA family, which can contain up to 1024 DSP slices [5]. The Xilinx[®] Spartan 3e (XC3S1600E-4FGG400C) has 36 dedicated 18-bit X 18-bit Hardware multipliers.

Digital Clock Managers

Digital Clock Managers (DCMs) are used for the generation of various clock signals derived for the external oscillator signal supplied to the FPGA. The DCM uses Delay-Locked Loops (DLLs) to provide frequency synthesis, clock skew reduction and control phase shift in clock signals within the FPGA. DCMs are regularly used to provide controllable clock signals of varying frequencies to various modules within the FPGA configuration. The Xilinx[®] Spartan 3e (XC3S1600E-4FGG400C) has 8 DCMs.

RAM blocks

Many FPGAs also contain dedicated Random Access Memory (RAM) blocks within their architecture. This feature allows for on-chip synchronous high-speed storage of large quantities of data. The Xilinx[®] Spartan 3e (XC3S1600E-4FGG400C) has 36 dedicated RAM Blocks, each with a capacity of 18 kBits, amounting to total of 360 kBits of storage.

Device Cost

As this project is being undertaken in conjunction with an industrial partner who plan to put this device into production once completed, cost is a major factor in the choice of FPGA to be used. As one would expect, higher-cost FPGAs are available with extensive resources, including millions of available programmable gates, extremely high operating speeds and numerous dedicated DSP and RAM blocks. Devices such as the Xilinx[®] Virtex7 range can have price tags in the region of many

thousands of euros. These would be prohibitively expensive for this project, making subsequent industrial implementation un-economical.

The Xilinx[®] Spartan 3e is a low cost, high performance, general purpose FPGA suitable for consumer-oriented applications. Xilinx[®] describes it as being “*specifically designed to meet the needs of high volume, cost-sensitive consumer electronic applications*” [2].

7.3.2 Power Supply

The circuitry of this system requires three voltage levels (3.3 V, 5 V and 12 V) to provide power to its various elements. Both the 5 V and the 3.3 V supplies are generated within the system from the external 12 V supply. The 12 V supply is required to provide a high current, in the order of 1 A, to power the antenna circuitry during tag activation. In addition, the 5 V and 3.3 V supplies are derived from the 12 V line. Therefore, 12 V power will be supplied by an external dedicated 12 V switch mode power supply capable of supplying up to 3 A. The Meanwell[®] S-25-12 12 V 25 W switching power supply [6] was suggested by this projects industrial partner. It has both the correct specifications and has been used by Dairymaster[®] within their systems for a number of years, proving to be both reliable and cost-effective.

The 3.3 V and the 5 V supplies are required to power the analogue filtering and amplification ICs, the ADC IC, all buffering ICs and the Enterpoint[®] Darnaw1 FPGA module, resulting in a relatively high current draw. A 3.3 V and a 5 V linear voltage regulator ICs were used to generate these supplies, from the 12 V supply provided to the board. The power supply to the Xilinx[®] Spartan 3e Starter Kit FPGA development board will be provided from the on-board voltage regulation via the supplied switch mode power supply. A reference ground will established between the Xilinx[®] development board and the Auto-ID reader board through connection of the ground planes via the FX-2 header.

As described in the section 7.7, the initial prototype system suffered from a large degree of self-generated EMI, which could clearly be observed on the system power lines. To reduce this EMI the use of a multi-layer Printed Circuit Board

(PCB) with split power and ground planes was used. Increased supply coupling to each IC was also implemented through the use of capacitive and inductive elements at close proximity to the power terminals of each IC.

7.3.3 Antenna Circuit and Power Amplification Stage

The antenna circuit of the system is identical to the design outlined in section 5.5.4 and used in the earlier Auto-ID reader module. The TTL level activation signal is provided directly from the FPGA via buffering and voltage level conversion circuitry, as in section 5.5.3.

7.3.4 Analogue Signal Conditioning

Two signal conditioning paths are required to accommodate the differing formats of the HDX and FDX tag signals. Both signal paths take their input directly from the antenna circuit, as shown in figure 7.4.

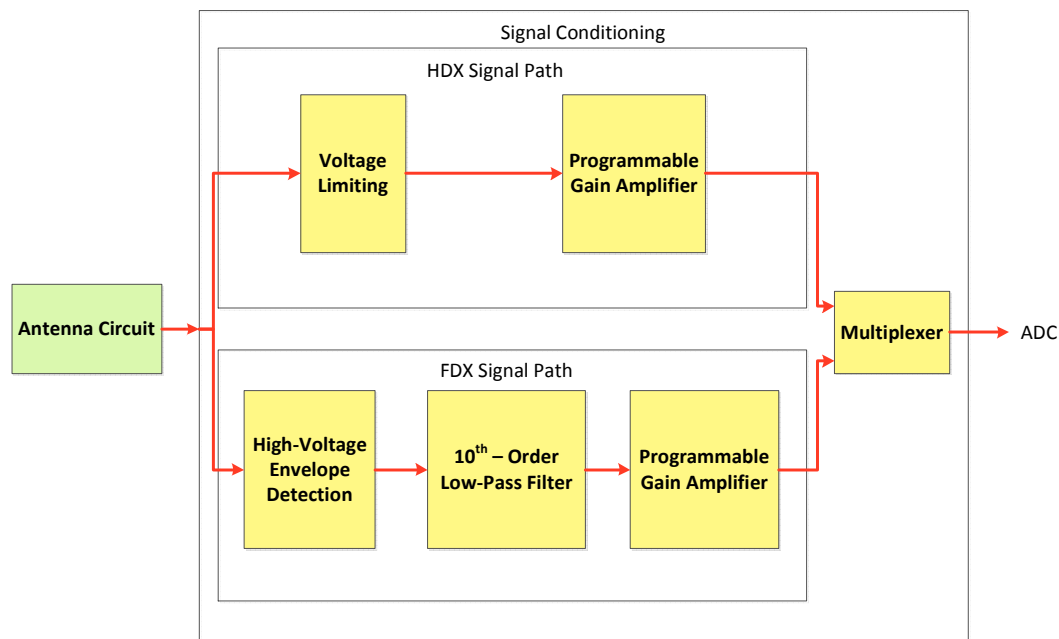


Figure 7.4: Block Diagram of Signal Conditioning Path

The first step in the HDX signal path is to limit the signal voltage as described in section 5.5.5. This isolates the sensitive analogue circuitry from the high-voltage activation signal on the antenna during the activation period. The low-level tag signal (during the listening period) is then amplified using a digitally controlled

analogue Programmable Gain Amplifier (PGA). This allows the FPGA-based digital system to control the gain applied to these signals, which allows these signals to be amplified to give the maximum signal amplitude presented to the ADC input, but ensures that the input does not become saturated. The Linear Technology® LTC6910-1 PGA [7] with 11 MHz Gain Bandwidth Product and Input Noise Down to 8nV/Hz was identified as a suitable PGA for this application. A 3-bit digital input driven from the FPGA is used to select between the PGAs gains of 0, 1, 2, 5, 10, 20, 50 and 100 V/V. The control of the PGA is discussed in section 8.5.4.

Within the FDX signal path a Low-Pass filter is required to remove the carrier wave, revealing the amplitude modulated Manchester encoded signal of the FDX tag. It was initially envisaged that all signal processing would be performed in the digital domain, on FPGA by digitising the FDX signal directly from the antenna circuit. As this signal has an amplitude in the order of 300 V_{p-p}, this is not possible with conventional ADCs.

One option investigated was to use a standard voltage divider circuit to reduce the received signal from its voltage approximately 300 V_{p-p} down to approximately 3 V_{p-p}. As the FDX Amplitude Modulated (AM) signal has an amplitude in the region of 20 to 40 mV_{p-p}, when divided by 100, this would become 200 to 400 μ V_{p-p}. As the ADC has an input range of 0 to 5 V (as discussed in section 8.5.3) and a resolution of 12 bits, resulting in a voltage interval of 1.2 mV per LSB. Therefore a 12 bit ADC would not have the required voltage resolution to be able to capture this signal effectively. If the resolution of the ADC was increased to 16 bits, this would provide a voltage resolution of 76.3 μ V, which is still too large to precisely represent the signal to be captured. ADCs of greater resolution with suitable specification proved to be beyond the budget constraints of this project.

Therefore a high-voltage envelope detector circuit was designed to reduce the activation signal component of the FDX signal to a more suitable level. This circuit took the form of a dual diode rectifier and a standard capacitor resistor envelope

detector circuit, as shown in figure 7.5. This circuit facilitates the extraction of envelope data within the range 2 to 20 kHz. The carrier waveform of 134.2 kHz will be greatly reduced.

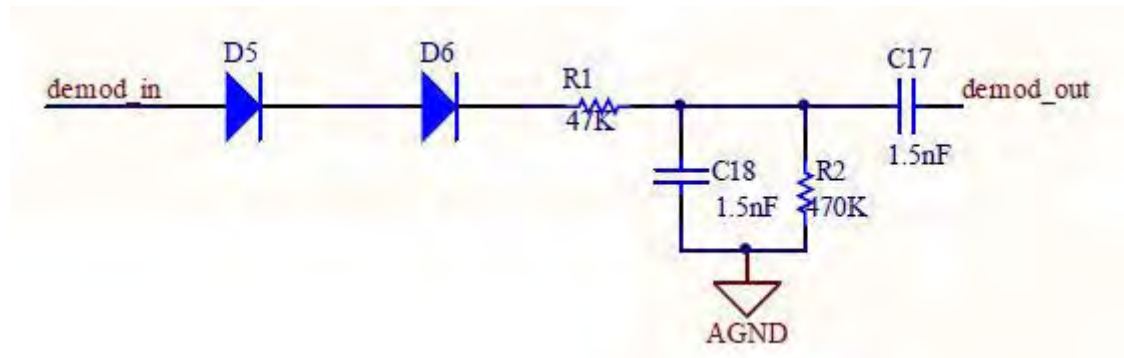


Figure 7.5: High-Voltage Envelope Detector Circuit

$$f_{CUTOFF} = \left(\frac{64kHz}{1,4,16} \right) \left(\frac{10k}{R_{EXT}} \right) = 19393.94Hz \quad (7.1)$$

An extremely steep roll-off at a cut-off approximately 20 kHz is required to remove the 134.2 kHz carrier signal from the received waveform. The Linear Technology® LT1569-6 [8] was identified as a suitable hardware programmable Low-pass filter IC. This IC provides a 10th order linear phase filter with a raised cosine amplitude response. The cut-off frequency of this filter can be configured using only a single resistor in accordance with equation 7.1 [8]. It was found that a 33 kΩ resistor will provide a cut-off frequency of 19,394 Hz. Once the carrier waveform has been removed from the received FDX signal, the Manchester encoded data stream is then amplified by a PGA for presentation to the ADC stage, via a multiplexer.

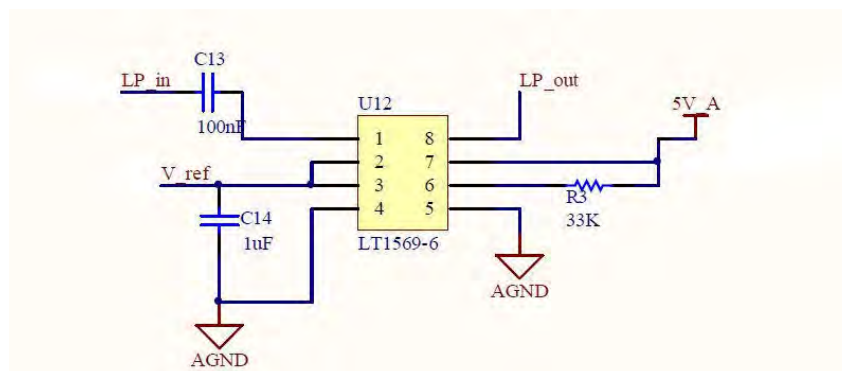


Figure 7.6: LT1569-6 Circuit Diagram

The final stage in the analogue signal conditioning is the use of an analogue multiplexer to toggle the input of the ADC between the FDX and HDX signal paths as appropriate. The state of this multiplexer will be controller directly from the FPGA.

7.3.5 Analogue to Digital Signal Conversion

The Auto-ID tag signal to be detected by this animal Auto-ID reader is within the frequency band 120-140 kHz. To implement advanced DSP algorithms for the filtering and subsequent demodulation of such a signal, a sampling rate much greater than the Nyquist frequency (double the signal frequency) must be implemented. A goal sampling rate of 10 Mega Samples Per Second (MSPS) was set for this system. This sampling rate is far in excess of the Nyquist criterion and will allow a high level of resolution in the frequency measurement of signals within the spectrum 120 kHz to 140 kHz. Due to the signal conditioning measures in place within this system to maximise the use of the ADC range, a medium resolution, 12-bit ADC over the range 0 – 5 V, is sufficient. This yields a voltage resolution of 1.22 mV.

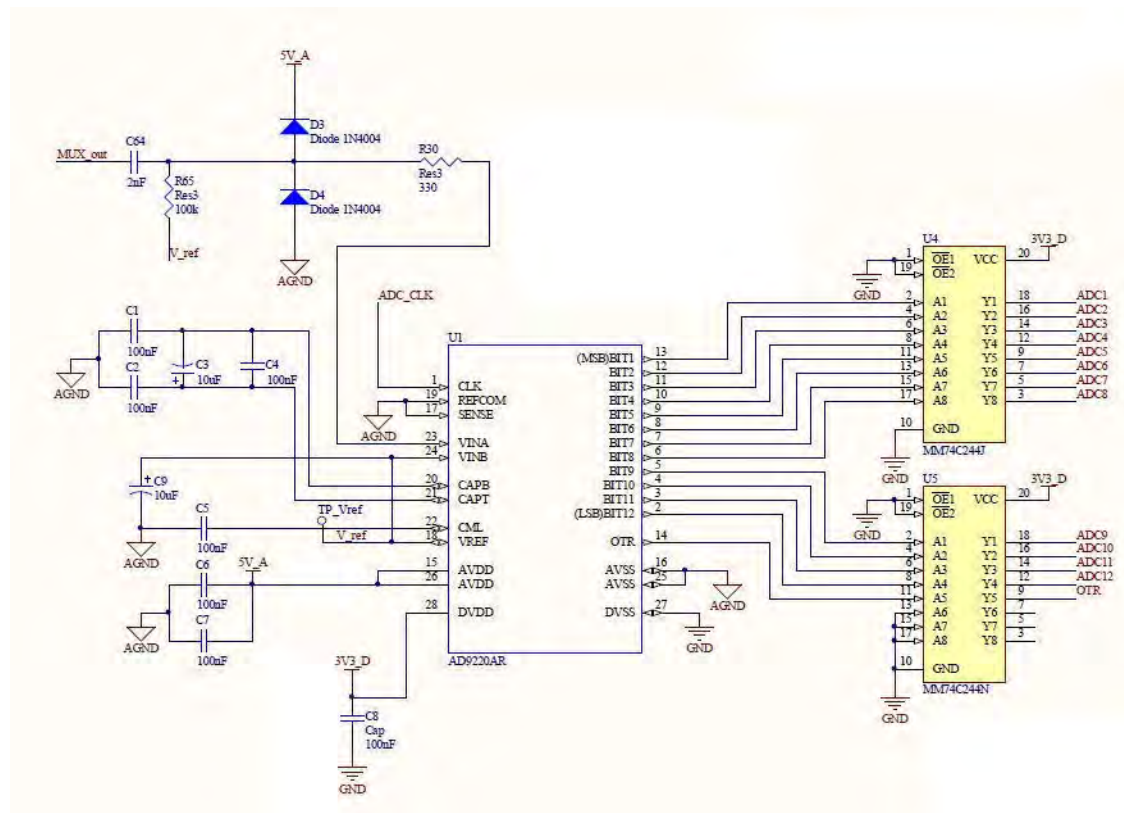


Figure 7.7: ADC Circuit Diagram

Signal digitisation is achieved using the Analog Devices[®] AD9220 [9] 12-bit pipelined Flash ADC which can operate at sampling rates of up to 10 MSPS. This device is pin compatible with a number of other ADCs in the Analog Devices[®] AD922x ADC family. This family offer ADC packages with sampling rates varying from 1.5 MSPS through to 40 MSPS. This device offers a resolution of 12-bits over a 5 V range, with integral and differential non-linearity's of less than half of one Least Significant Bit (LSB).

7.4 On-FPGA Hardware Description

The complex digital system to be configured on the target FPGA is composed of a system of discrete digital modules, each performing a vital function within the design. These modules are then integrated into a single system through the use of a top level control and integration module. These modules have been created using the VHDL Hardware Description Language (HDL) using both architectural and behavioural descriptions.

This VHDL system was designed using the Xilinx[®] ISE Electronic Design Automation (EDA) tools. The VHDL systems developed has been extensively tested by simulation using the Xilinx[®] ISim HDL simulation tool in advance of FPGA configuration and system implementation.

Figure 7.8 shows a block diagram of the internal modules of the FPGA hardware system. A logic control block controls the synchronisation of the system components and also forms the input/output interface to the control section of the design. The Activation Signal Generation module provides the TTL driver signal for the activation signal power stage. The ADC Control module provides the sampling control signal for the ADC. The resulting 12-bit sample from the ADC is then presented to the DSP module for processing and the RAM module for storage. After DSP processing the data is ready for demodulation and the resulting bit-stream is presented to the Logic Control module for transmission to the host device. Each module of the system will now be discussed in more detail. All VHDL files are presented in Appendix A.7.

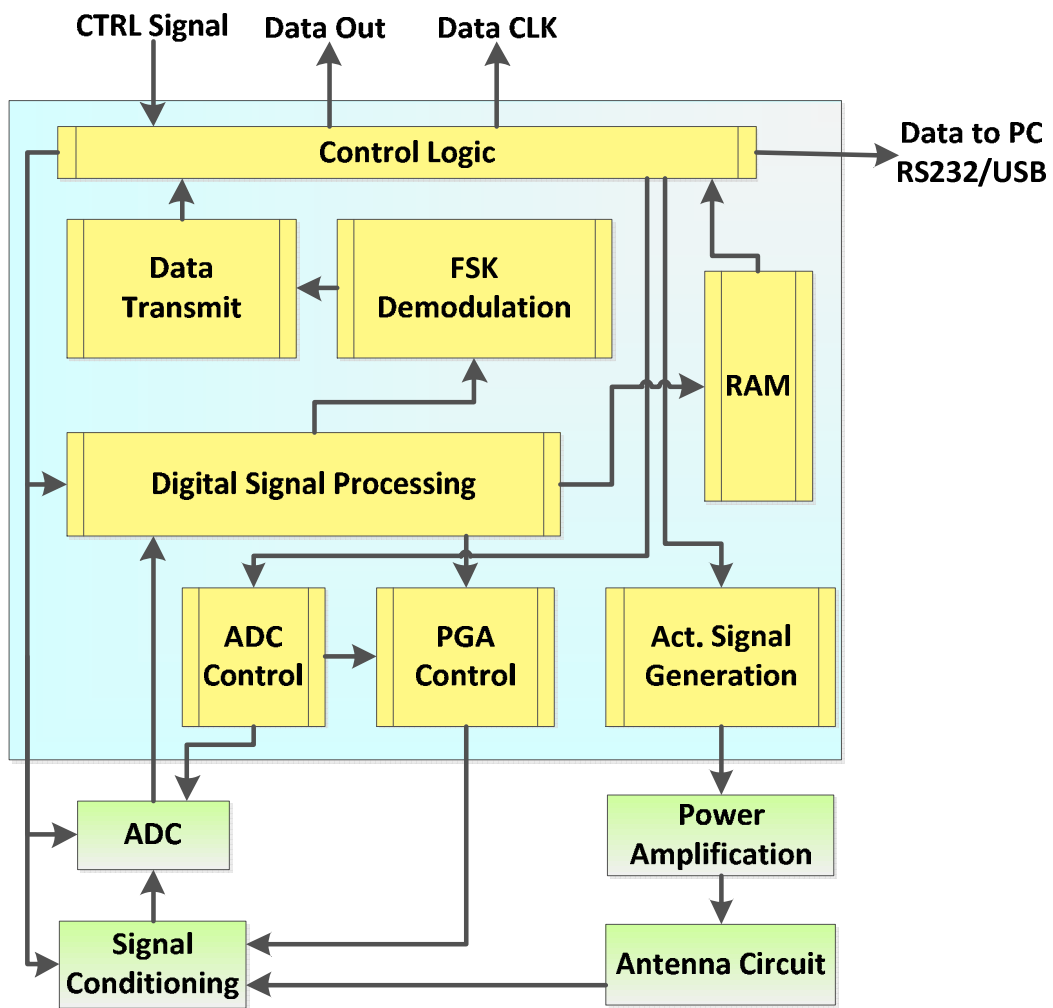


Figure 7.8: Block Diagram of the FPGA Internal Modules

7.4.1 Top Level System Integration and Control

For this system to operate as designed, it is vital that a control module be instantiated to synchronise the various discrete modules of the design. This section of the system encompasses the module interconnects, as well as the assigning of external signal connections and also performs the top level control of the system.

Device synchronisation takes the form of a timing protocol outlined in the ISO standardisation documents. The activation signal must be generated for 50 ms, during which a FDX signal may be received. Following this, the activation signal is ceased and a 50 ms listening period is observed for reception of the HDX tag response. Synchronisation is controlled externally by the animal Auto-ID system

control board and is distributed to the relevant VHDL modules by this control module.

All inter-module control signals, clock signals and data buses are implemented as standard logic vectors to allow compatibility between the various module architectures.

7.4.2 Activation Signal Generator

The required activation signal is generated by dividing a 17.1776 MHz clock source by 128, resulting in a 134.2 kHz waveform. This is achieved through the use of a rise-edge triggered binary 8-bit counter, with the Most Significant Bit (MSB) of the counter output generating the output waveform. The result is a toggling of the output, for each 128 rising-edges of the 17.1776 MHz clock signal.

The 17.1776 MHz signal is not a standard crystal value and, as such, a specialised crystal was manufactured. The clock input of the FPGA requires a TTL level clock signal, which cannot be fulfilled by a crystal resonator. Therefore a standard crystal oscillator circuit was designed, using a Schmitt-trigger inverter to provide the TTL level signal.

7.4.3 Analogue-to-Digital Conversion Control

The ADC is intended to digitise the incoming Auto-ID tag signal present on the antenna circuit at a rate of 10 MSPS during the HDX tag listening period. Therefore, during the HDX listening period, a 10 MHz sample control signal will be required to drive the ADC. This signal can be taken directly from the DCM within the FPGA. Sampling does take place during the HDX activation period. Therefore a control signal from the Logic Control block is used to synchronise the ADC data capture with the Activate/listening cycles of the reader.

7.4.4 Programmable Gain Amplifier Control

Both PGAs require a 3-bit digital control bus. Two 3-bit up/down counter are instantiated in VHDL to provide this 3-bit output. The gain generated by the PGA

must be sufficient to maximise the use of the input range of the ADC, but avoid saturating the ADC input.

To provide intelligent PGA control, each time a tag response is detected, a sample of the amplitude of the received response is made by the DSP module and passed to the PGA control block. Based on this amplitude reading, the up/down counter is incremented or decremented accordingly, to augment the gain of the PGA for the subsequent tag reading. This allows the full range of the 12-bit ADC to be used efficiently. Signal headroom of 10% (0.5 V) is always provided to allow for slight variations in the received signal amplitude without input saturation.

7.4.5 Digital Signal Processing Module – Bandpass Filter

The DSP element of this initial FPGA based Auto-ID system is comprised of a steep roll-off digital filter with a pass-band of 120 to 140 kHz. The use of a Finite Impulse Response (FIR) digital filter in the signal conditioning of an animal Auto-ID tag signal was demonstrated successfully in Case Study 3. Initially an FIR digital filter design was proposed for use within this DSP-based Auto-ID reader. In the prototype MATLAB[®]-based reader, the design required a 3000th order FIR filter to achieve the required level of roll-off outside of the pass band of 120-140 kHz.

It is envisaged that the filtering algorithm for this system to be implemented in parallel as opposed to the sequential multiply accumulate operation as implemented in the MATLAB[®] based Auto-ID reader. Within a real-time embedded system it would not be feasible to implement a 3000 order filter on a low to medium cost FPGA, due to the limited amount of hardware multiplier units available on such FPGAs. Therefore a reduced order FIR filter was designed. As the chosen FPGA, the Xilinx[®] Spartan 3e (XC3S1600E-4FGG400C), has 36 dedicated 18-bit by 18-bit two's complement multipliers, a FIR filter of up to 36th order could feasibly be implemented.

A number of FIR filter were designed using the MATLAB[®] Filter Design Toolbox and were tested within the MATLAB[®] prototyping environment to

evaluate their performance. When presented with signals representative of signals which would be received from an Auto-ID tag it was found that these filters were insufficient to perform the filtering required.

Infinite Impulse Response Digital Filter Development

An alternative to FIR filters is the Infinite Impulse Response (IIR) filter. In comparison to FIR filters, IIR filters can often achieve steeper roll-off using lower orders due to the recursive nature of the IIR filter transfer function, shown in equation 7.2. This steeper roll-off often comes at the price of increased filter instability. These filters are often implemented in digital hardware, using hardware multiplier and adders, in the format shown in figure 7.9.

$$y_n = \frac{1}{a_0} \left(\sum_{i=0}^P b_i x[n-i] - \sum_{j=1}^Q a_j y[n-j] \right) \quad (7.2)$$

The IIR filter design algorithms used within the MATLAB[®] filter design environment have a requirement that the term ‘a₀’ of an IIR filter has a unity value, as shown in figure 7.9. Alteration of this coefficient from a unit value has the effect of destabilising the filter. Therefore the other coefficients within the designed filter cannot be scaled to integer values as is common practice with the implementation of FIR filters. Therefore, decimal representations of the coefficients must be used. In the field of embedded DSP, two main conventions are used for the representation of decimal numerical values; Fixed-point and Floating-point arithmetic. Therefore it was required to use either fixed-point or floating-point arithmetic to achieve the accuracy required by this system, neither of which are standard features of VHDL.

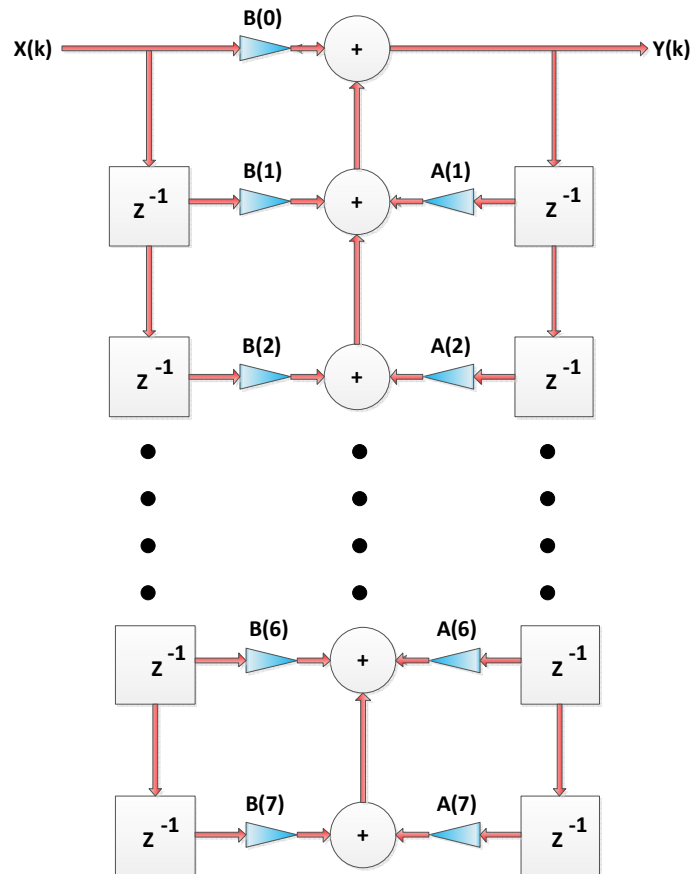


Figure 7.9: IIR Filter Architecture

The VHDL fixed-point library currently recommended for use with Xilinx[®] EDA tools is fixed_pkg.vhdl. This library has yet to be standardised by the IEEE and, as such, is a work in progress. It is being developed by David Bishop of VHDL.org [11]. The current version of the Xilinx[®] ISE 12.3 has this fixed-point arithmetic library bundled with it but is listed as “IEEE Proposed” and is not automatically included in the project library as other, IEEE approved, libraries are.

A number of 8th and 10th order IIR bandpass filters were successfully designed in the MATLAB[®] prototyping environment using the filter design toolbox. A sampling frequency of 10 MSPS was specified along with a pass-band of 120 kHz to 140 kHz, with suitably large roll-off of 80 dB/Decade in the stopband.

IIR Filter Coefficient Quantisation

MATLAB[®] uses 64-bit floating point arithmetic within its filter design toolbox. In order to operate successfully in a VHDL implementation the coefficients of the

filter need to be truncated to suit the bit-width of the available dedicated hardware multipliers on the target FPGA device. In this case the target device is the Xilinx[®] Spartan 3e (XC3S1600E-4FGG400C) which incorporates 36 18-bit X 18-bit dedicated hardware multipliers. Therefore the coefficients of the filter must be quantised to 18-bit representations in order to use only a single multiplier for each multiplication.

The IIR filter, being a recursive filter, does not respond well to coefficient quantisation. The round-off error introduced by coefficient quantisation is fed back into the system which results in the compounding of the error. The result is that the rounding of the IIR coefficients from the 64-bit coefficients generated by the MATLAB[®] Filter Design Toolbox to 18-bits greatly changes the frequency response of the IIR filter. In fact the resulting frequency response often bears no resemblance to the intended frequency response of the designed filter. Figure 7.10 shows the intended frequency response of the filter design within the MATLAB[®] Filter Design Toolbox and implemented in MATLAB[®] using 64-bit fixed-point arithmetic. Figure 7.11 shows the same filter, implemented in MATLAB[®], but this time with the filter coefficients truncated to 18-bit fixed-point numbers.

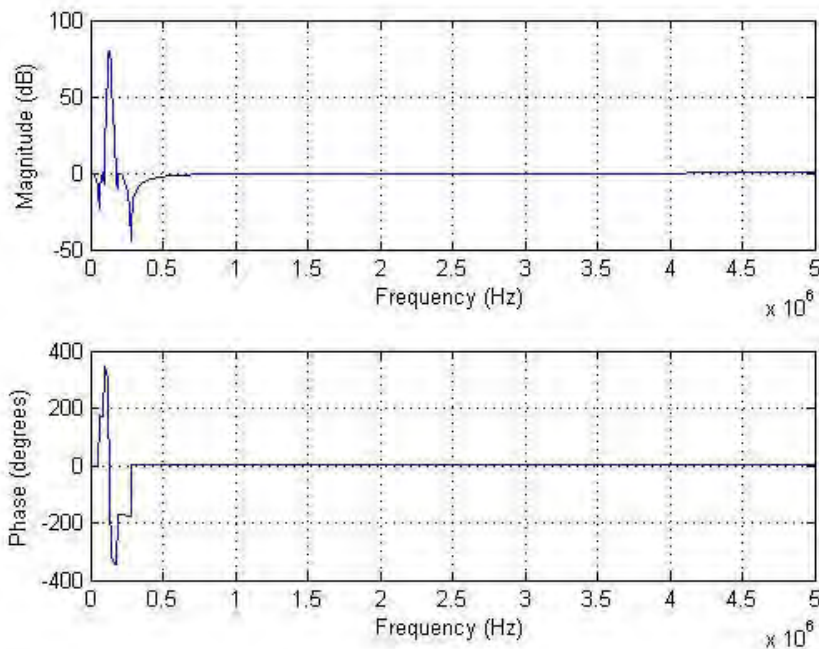


Figure 7.10: 64-Bit IIR Filter Frequency Response

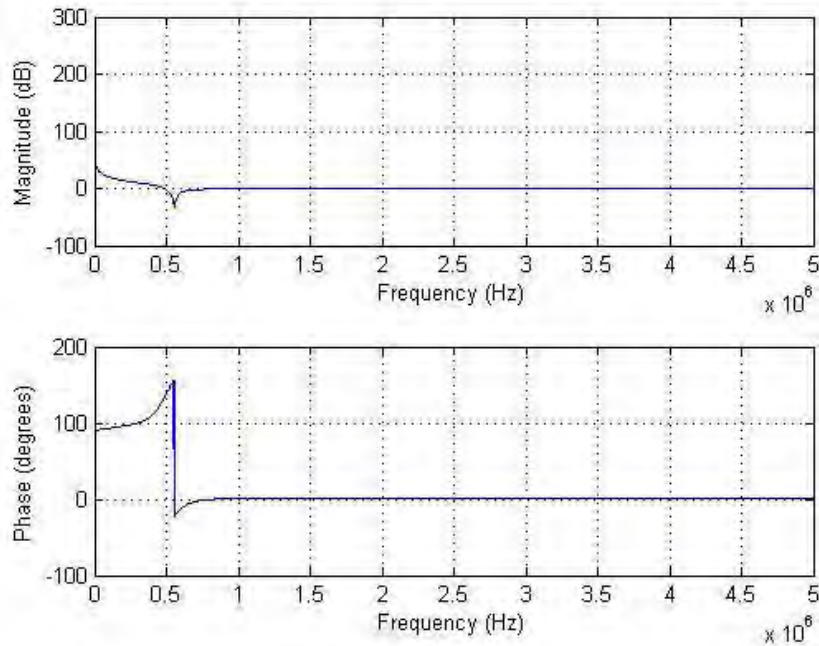


Figure 7.11: 18-Bit IIR Filter Frequency Response

Further investigations found that this change in the filters frequency response is more extreme in higher-order IIR filters, with lower order filters being relatively unaffected. Continued investigation found that if a high-order filter can be reduced to a cascaded series of lower-order filters, the effects of round-off error can be greatly reduced. Therefore the 8/10 order filters designed were redesigned as a cascaded series of 2nd order IIR filters, a technique referred to as a Second Order System (SOS), as in figure 8.12. These SOS filter ‘blocks’ were then implemented in MATLAB[®] in Direct Form I with truncated 18-bit coefficients and cascaded to form the required IIR 8th/10th order IIR filter.

The coefficients of these SOS blocks were then manually converted to 18-point fixed-point binary two’s complement numbers for use in the implementation of an embedded IIR filter. The system was then simulated using the bundled Xilinx[®] testbenching tools. Stimulus waveforms were developed to emulate the sinewaves of various frequencies with the output of the system examined with reference to the desired frequency response of the filter.

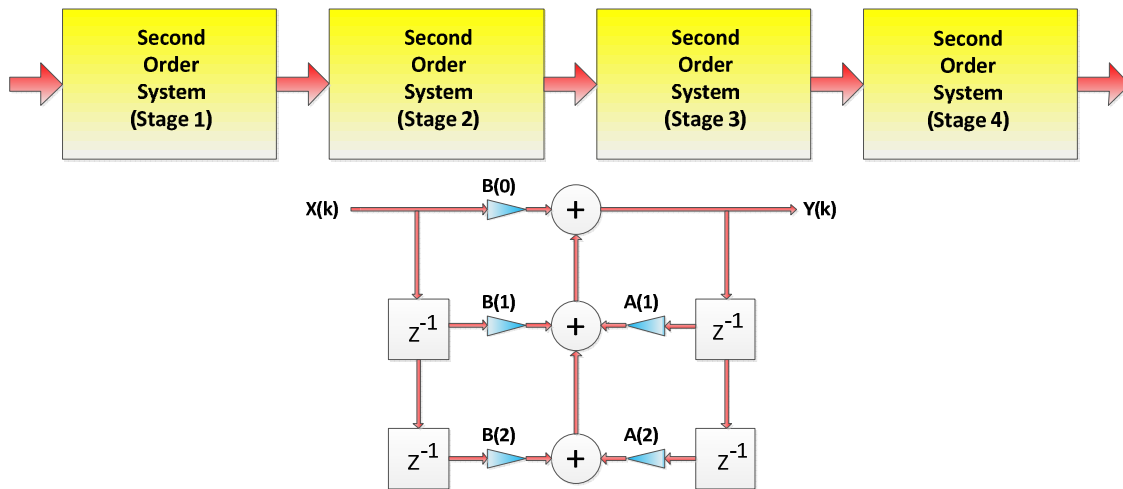


Figure 7.12: Second Order System IIR Block Diagram

Signal Scaling within the IIR Filter

A problem arose with the saturation of the 18-bit signals within some of the SOS filter stages. A large gain is applied during certain SOS IIR stages for pass-band signals. The result is that the magnitude of the signals becomes too large for the internal 18-bit fixed-point signals to represent, resulting in saturation of the 18-bit signal. One option to overcome this saturation is to upgrade the fixed-point signals to bit-widths greater than 18-bits. For this implementation, this would be undesirable as the internal hardware multipliers of the Xilinx[®] Spartan 3E FPGA operate as 18-bit x 18-bit multipliers. If signals of greater than 18-bits in length are to be multiplied by the system, the number of hardware multipliers required for each multiplication will have to be doubled, along with additional circuitry to allow these two multipliers to act as a single larger bit-width multiplier. As the Spartan 3e (XC3S1600E-4FGG400C) only contains 36 dedicated hardware multipliers, the number of IIR SOS stages which can be implemented within the FPGA will also be reduced.

A more suitable option to overcome this problem was found through the use of predefined input scaling to each stage of the SOS, as shown in figure 8.13. The scaling chosen was based on the maximum gain within that block and the maximum fixed-point number which could be represented by that block's internal signals while allowing maximum accuracy and precision. Each scaling factor was

chosen as a power of 2 to allow efficient bit-shifting divisions. Testing proved that, with these pre-scaling factors inserted in advance of each SOS block, no saturation occurs.

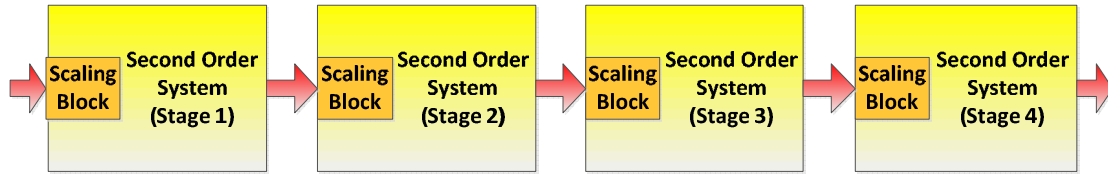


Figure 7.13: SOS IIR System with Scaling Blocks

The transient response of each IIR filter was analysed and found to be acceptable. The frequency response of the resulting SOS IIR filter matched the intended frequency response as shown in figure 7.14. It is clear from this figure that the desired filter characteristics have been retained during implementation. The IIR filter was also rigorously tested for stability and saturation of internal signals with ‘worst case scenario’ filter inputs and found to operate as designed.

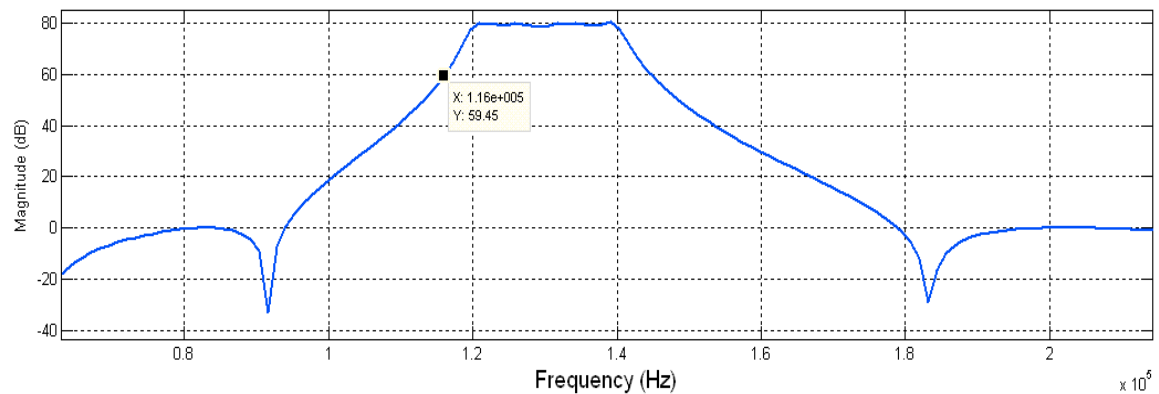


Figure 7.14: Second Order System IIR Filter Frequency Response

7.4.6 RAM Module

Xilinx[®] FPGA devices contain dedicated RAM modules within their hardware architecture. The Xilinx[®] Spartan 3e (XC3S1600E-4FGG400C) contains 36 such modules, each containing 1024 18-bit addressable memory locations for a total of 36864 addressable memory locations. These RAM blocks are instantiated using the

Xilinx® Core Generator tools included in the Xilinx® ISE EDA tools. Each RAM block is instantiated individually with VHDL code and all 36 must then be combined to create a single block of 36864 memory locations.

The RAM interface takes the form of a Device Enable, a Write Enable, a Clock Input, a 16-bit data input port and a 2-bit parity data input port, a 16-bit addressing port and a Synchronous Set/Reset pin. This RAM module is intended to capture a stream of 36864 sequential 16-bit numbers, directly from the output of the DSP block. Therefore the addressing during a write operation will always be sequential from 0 to 36864. This allows a simplified addressing mechanism which would cycle from addresses 0 to 36864 and output a ready flag once the memory is fully populated.

The 16-bit address is generated from a 16-bit up-counter with extra combinational logic to cause a reset and a flag when 36864 has been reached. The 10 least significant bits are used to index the individual 16-bit memory locations within the RAM block. The 6 most significant bits are used to index the RAM blocks (1 to 36). The RAM block indexing section takes the form of two thirty six-way 16-bit hardware multiplexers, one for memory write functions and one for memory read functions.

The clock signal to drive this counter is taken directly from the ready flag of the DSP block. Once a sample has been processed by the DSP block and the DSP blocks output is valid, the rising edge of the ready flag will trigger the address counter to increment to the next memory location. The ready flag of the DSP block is configured as a short pulse, meaning the falling edge of this pulse can be used as a write command for the RAM block. Such a pulse, with suitable duration, allows the counter to increment and the memory address to become valid before the write command is given.

Once the RAM module has been fully populated with data from the DSP block, it can be accessed by the Universal Asynchronous Receive/Transmit (UART) module, found within the control module, to transfer this data to the PC for

examination. Once a data request is received from the PC, the UART requests data from the RAM module, which is set to read mode and the addressing module is triggered to cycle from 0 to 36864.

7.4.7 FSK Demodulator

The FSK demodulation algorithm used in this design is similar to that described in section 6.3.5 of this thesis. Firstly a frequency counter is used to ascertain the instantaneous frequency of each cycle of the signal. The sign-bit of the each Two's complement sample is used to discriminate between positive and negative samples and hence locate the zero-crossing points of the signal. Once the zero-crossing point is identified, the number of samples between each zero-crossing is used to generate an accurate representation of the signals instantaneous frequency.

As before, the signal is then analysed to detect sequences of 16 cycles of the same frequency, in accordance with the FSK demodulation scheme, where each bit is represented by either 16 cycles of 124.2 kHz or 134.2 kHz.

7.4.8 Universal Asynchronous Receiver/Transmitter

A Universal Asynchronous Receiver/Transmitter (UART) is required within this project to allow the analysis of both the digital signal captured by the ADC and the digital signal resulting from the application of the DSP algorithm. It will allow the serial transmission of data from the FPGA to the PC for further analysis. The Xilinx[®] Spartan 3e Starter Kit FPGA development board contains all the necessary external hardware to create a RS232 connection from the reader to the PC, i.e. a voltage level translator and an RS232 DTE style connector. The Enterpoint[®] Darnaw 1 module does not contain this hardware and therefore it was required to include them on the final printed circuit board. A standard RS232 style UART VHDL module was created to convert the parallel 16-bit data stored in RAM to 115200 BPS serial data and output this serial signal to the voltage translator for transmission of RS232.

7.4.9 Digital Clock Manager

The FPGA is provided with a 50 MHz clock signal from an external oscillator circuit present on both the Xilinx[®] Spartan 3e Starter Kit FPGA development board and the Enterpoint[®] Darnaw1 module. The Xilinx[®] Spartan 3e (XC3S1600E-4FGG400C) contains 8 dedicated DCMs. One of these DCMs is configured using the Xilinx[®] ISE EDA tools to synthesis both a 100 MHz and a 10 MHz TTL clock signal. The 100 MHz clock signal is used to drive the FPGA DSP and RAM blocks and also used within the Logic Controller block. The 10 MHz clock is provided to the ADC control section for control of the ADC sampling rate and to other module for the purpose of synchronisation.

7.5 Advanced DSP Algorithms for Animal Auto-ID Systems in High EMI

The EMI present in a dairy parlour has been analysed and categorised in section 6.2. It was noted that while ‘Bursty’ type EMI plays a major role in reduced performance of animal Auto-ID systems, it can often be located and eliminated at source due to its localised nature. This has led to investigations into advanced DSP algorithms to allow the operation of animal Auto-ID systems in the presence of high levels of ‘Continuous’ type EMI.

A novel system has been devised which evaluates the EMI present and instantiates a suitable filtering and demodulation algorithm which can operate under the observed EMI conditions. In the case of a single narrowband interferer signal, a system has been devised which effectively ignores the signal frequency components relating to the interferer to allow accurate demodulation of the tag signal. To allow for instances where multiple, or wider bandwidth continuous interferers are present, a novel system is presented which analyses the interference pattern created between the interferer signal and the tag signal to allow accurate demodulation.

7.5.1 EMI Analyser – Dual Band

Firstly the profile of EMI within the reader environment must be analysed. As the data processing resources available on-FPGA are limited, a much more simplistic version of the system developed in section 6.2 will be developed here. As an FSK-based data transmission system can be divided into two discrete FSK frequency bands, the profile of any narrowband EMI which may affect such a system can be simplified into EMI power measurements of these two separate frequency bands.

A reconfigurable IIR filter is created, similar to that designed in section 7.4.5. The hardware implementation of an IIR filter takes the form of a series of hardware multipliers and registers. Each hardware multiplier takes as its input a digital number from the input/output delay register and a filter coefficient. Therefore a filter can be reconfigured to a different frequency response by simply changing the coefficients in the filter coefficient array. In this way a reconfigurable IIR filter can be created by simply de-multiplexing two or more coefficient arrays to the coefficient ports of the IIR filter hardware multipliers. The appropriate filter can then be chosen and implemented by applying the correct code to the de-multiplexer.

Two 8th order SOS IIR bandpass filters were designed in the MATLAB[®] Filter Design Toolbox, the first with a passband of 120-130 kHz and the second with a passband of 130-140 kHz. The coefficients of the designed filters are then placed in two separate filter coefficient arrays. A de-multiplexer is used to select which set of coefficients is to be used.

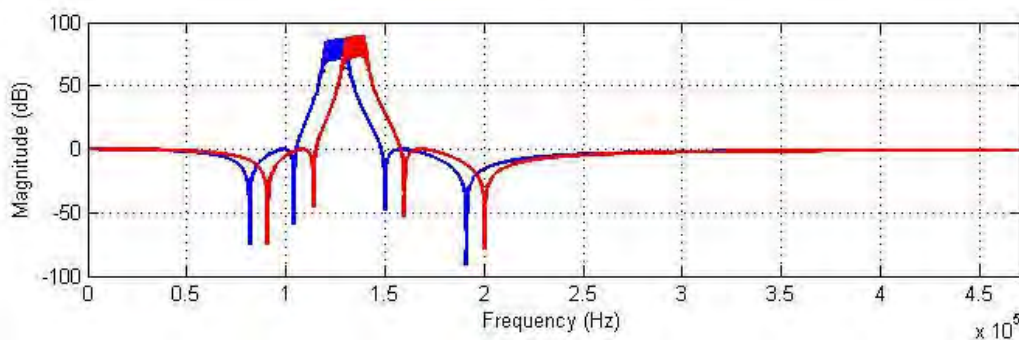


Figure 7.15: Dual-Band EMI Analyser Frequency Response

On start-up of the Auto-ID system, each filter is implemented for a predefined time suitable for characterisation of the EMI present. Experimentation found that 10 ms was a suitable duration. The EMI in each frequency band is then characterised by finding the power and maximum amplitudes of the signals. These measurements are then used to tell whether the EMI is ‘bursty’ or ‘continuous’ in nature and which FSK band is affected. Based on this evaluation the most suitable DSP algorithm can be set in place, as shown in figure 7.16.

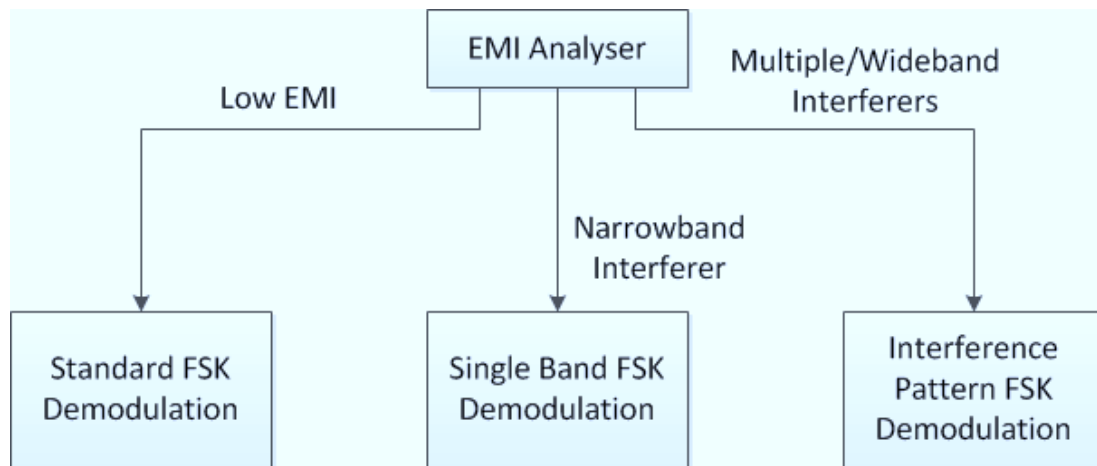


Figure 7.16: Demodulation Algorithm Instantiation

7.5.2 Single-Band FSK Demodulation

Hypothesis

As noted during the investigation and characterisation of EMI in the LF band, EMI in the lower frequency range often have the characteristic of a ‘continuous’ narrow-bandwidth interferer. As already described, HDX animal Auto-ID systems operate using a FSK system operating at the discrete frequencies of 124.2 kHz and 134.2 kHz. If an EMI signal has a sufficiently narrow bandwidth, it will often affect only a single frequency band used in the FSK modulation scheme.

An FSK signal can be demodulated based on the presents or absence of a signal of a particular frequency. Therefore only a single frequency band (120 kHz to 130 kHz or 130 kHz to 140 kHz) need be monitored and the other discarded. The

choice of which frequency band to monitor can be made based on which frequency band contained the lowest levels of EMI as measured by the in-system EMI analysis tool.

Implementation and Evaluation

Firstly a reconfigurable 8-th order IIR filter is instantiated as in section 7.5.1. The choice of whether the 120 kHz to 130 kHz or the 130 kHz to 140 kHz bandpass filter is implemented is made based upon the spectral components of the interferer signal detected by the EMI analyser. Once the correct IIR filter is implemented, the tag signal is processed by the chosen IIR filter. Once filtered, the resulting signal contains only one of the discrete FSK frequency component of the tag signal, with the EMI signal and the other discrete FSK frequency component removed. This signal can then be demodulated by identifying the presence and absence of the FSK signal and relating that to an appropriate data bit.

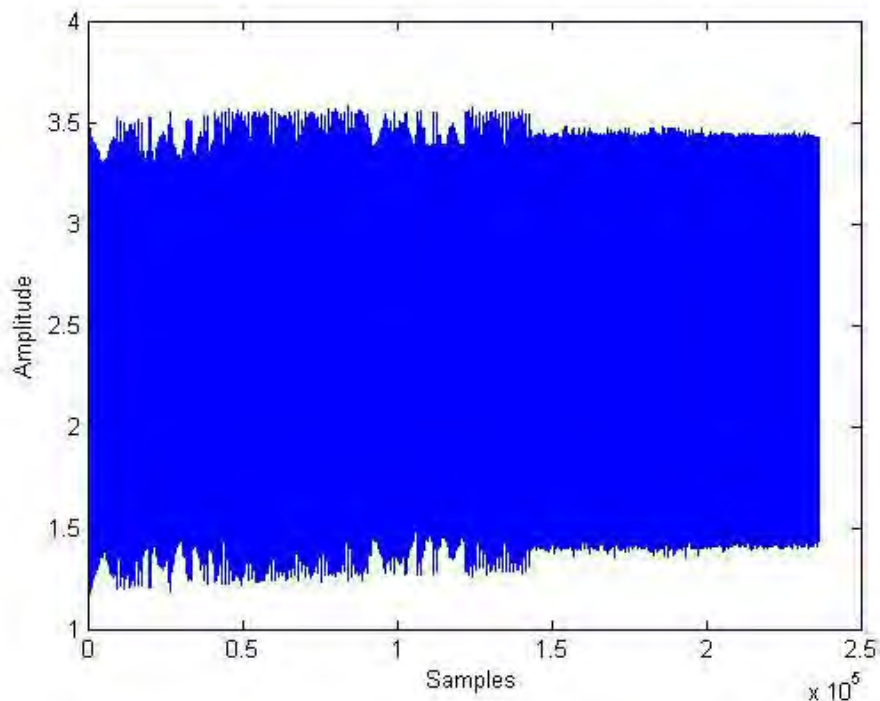


Figure 7.17: Tag Signal in High Level EMI

Figures 7.17 and 7.18 demonstrate the effect of this operation, where figure 7.17 is a data capture of a tag response signal in the presence of severe EMI of frequency 125 kHz. The 125 kHz interferer signal had been identified by the EMI

analysis tool, resulting in the instantiation of the 130 kHz to 140 kHz passband IIR filter. The result of this filtering is shown in figure 7.17. Here the tag signal is clearly seen, with the 134 kHz sections (representing a binary ‘0’) amplified and the 124.2 kHz (representing a binary ‘1’) and the 125 kHz interferer removed from the signal. The signal can now be demodulated by using a standard frequency counter method to identify ‘0’s and using the absence of a signal above a predefined threshold as an indication of a binary ‘1’.

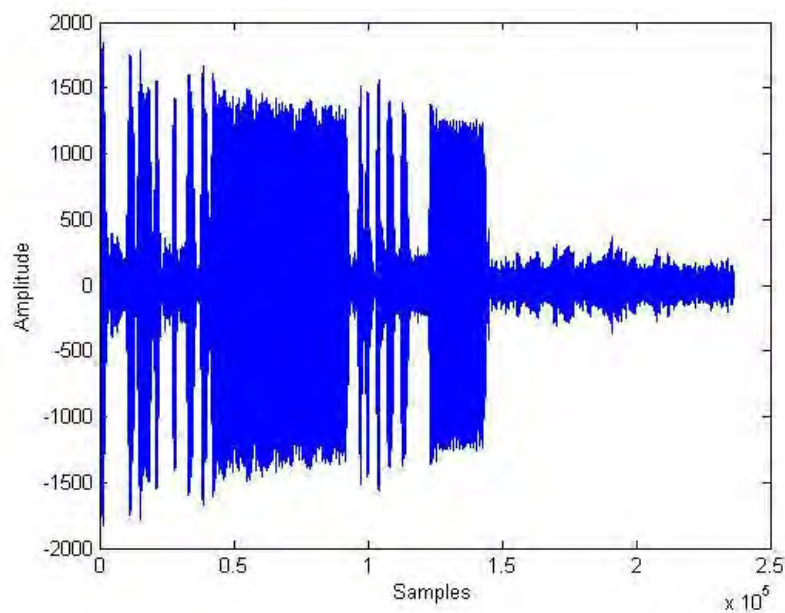


Figure 7.18: Filtered Tag Signal

7.5.3 Interference Pattern-Based Demodulation

Hypothesis

In areas which suffer from multiple narrowband interferer signals, there may be interferer signals in both discrete FSK frequency bands. In such a situation the algorithm described in section 7.5.2 would not allow successful tag signal demodulation.

Basic wave theory tells us that when two or more signals meet at a point they become superimposed upon one another, resulting in a single waveform equal to the vector sum of the incident waves. This phenomenon is known as interference,

which can take the form of constructive or destructive interference, depending on the phase angle between the interfering waveforms. When waveforms of different frequency meet, their phase angle is constantly changing, leading to an oscillation between constructive and destructive interference, often referred to as an interference pattern. This forms a signal envelope, as shown in figure 8.19 This also applies to the interaction between an animal Auto-ID signal and a continuous EMI signal. Therefore, when it is not possible to remove an interferer signal by filtering due to the interferer being present in both FSK frequency bands, it may be possible to identify the presence of a tag signal by analysing the received signal for changes in the interference pattern.

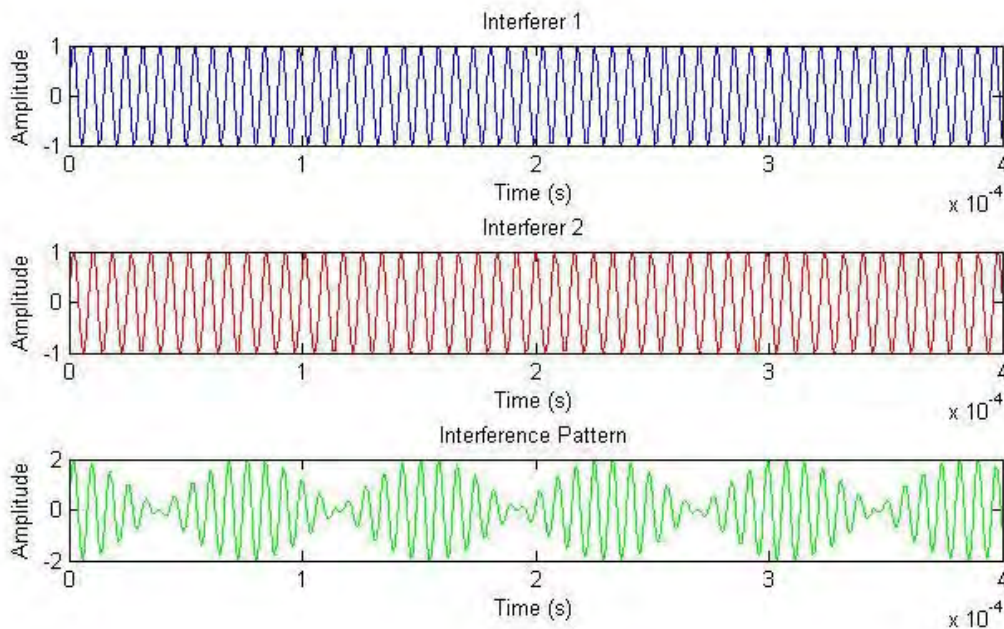


Figure 7.19: Basic Interference Pattern between Incident Waveforms

As both the 124.2 kHz tag signal representing a ‘1’ and the 134.2 kHz tag signal representing ‘0’ will cause the creation of similar interference patterns, more in-depth analysis is required to differentiate between which frequency tag signal is causing the interference pattern at a given location in the received signal. This can be achieved by filtering the received signal with a bandpass filter of either 120 kHz to 130 kHz or 130 kHz to 140 kHz pass band, thus removing the interference effects of one of the tag FSK signals. Again, the choice of which frequency band to

monitor can be made based on which frequency band contains the lowest levels of EMI as measured by the in-system EMI analysis tool.

Once filtered, the resulting signal has two distinct parts, one which is almost identical to the EMI present within the frequency band of interest when no tag signal is present and a second which represents an interference pattern due to the presence of one of the FSK tag signals (124.2 kHz or 134.2 kHz), the other FSK signal having been removed by the filter.

By then extracting the interference pattern envelope a clear indication of the where the isolated FSK tag signal ('1' or '0') is present, leading to the demodulation of the animal Auto-ID signal.

Implementation and Evaluation

When multiple narrowband high level EMI signals, affecting both FSK bands, are identified by the EMI analysis tool, the interference pattern based demodulation scheme is implemented. Firstly a 120 kHz to 130 kHz or 130 kHz to 140 kHz 8th order bandpass IIR filter is instantiated, as designed in section 8.5.2. The decision upon which IIR filter should be dynamically implemented is again based on which frequency band has the lowest EMI level, as assessed by the on-board EMI analysis tool.

To isolate and analyse the resulting interference pattern the LF envelope must be extracted from the signal. A Hilbert transform is an accepted DSP method for capturing the envelope of a signal to extract the lower frequency ripple in the carrier signal [12]. Due to the limitations of the resources available within the FPGA, it was not possible to implement the Hilbert transform, so an approximation of this transform was needed. In analogue systems, an enveloped detector consists of a simple rectifier circuit, to remove the negative elements of the signal, followed by a low-pass filtering section. In the digital domain this operation can be implemented by finding the absolute magnitude value of each data point, analogous to the analogue rectification process, and then low-pass filtering the result. The

low-pass filter is implemented with an 8th order IIR filter with a 20 kHz cut-off frequency, created in the same manner as those created in section 7.4.5.

Once the envelope signal of the interference pattern has been extracted, demodulation is achieved by noting the instantaneous amplitude of the envelope and comparing this to the envelope amplitude observed at a time when a tag signal is not present and only the EMI signal is present. By associating the result of this comparison with the duration of the bit period, the bit-stream can be extracted.

Figure 7.20 shows a received tag signal in the presence of two interferer signals, one at a frequency of 122 kHz and the other at 137 kHz. As the 122 kHz EMI was found to be of slightly lower magnitude, the 120 kHz to 130 kHz bandpass filter was implemented.

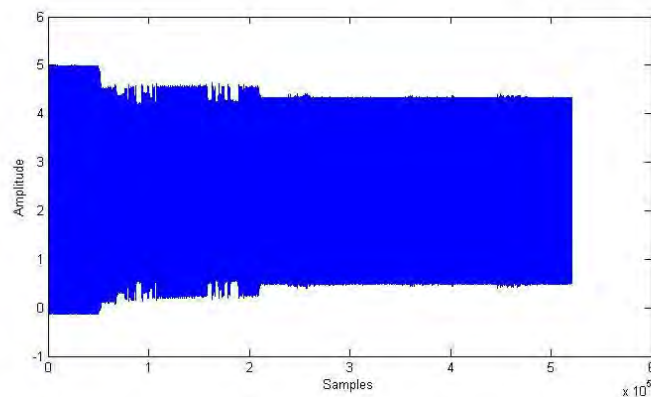


Figure 7.20: Tag Response in Dual-Frequency EMI

The remaining signal is comprised of the 124.2 kHz tag signal representing ‘1’s and the interferer signal present in the 120 kHz to 130 kHz band. The 134.2 kHz tag signal representing ‘0’s and any interference pattern present outside of the 120 kHz to 130 kHz band have been removed. At this point the peaks of the interferer signal can be clearly seen, as in figure 7.21. The high magnitude ripple (peaks and troughs) represents a binary ‘1’, as the 124.2 kHz tag signal is causing an interference pattern with the 122 kHz EMI signal. The lower magnitude ripple section represents a ‘0’, as the 134.2 kHz has been removed through the filtering process and is therefore no-longer interacting with the 122 kHz EMI signal.

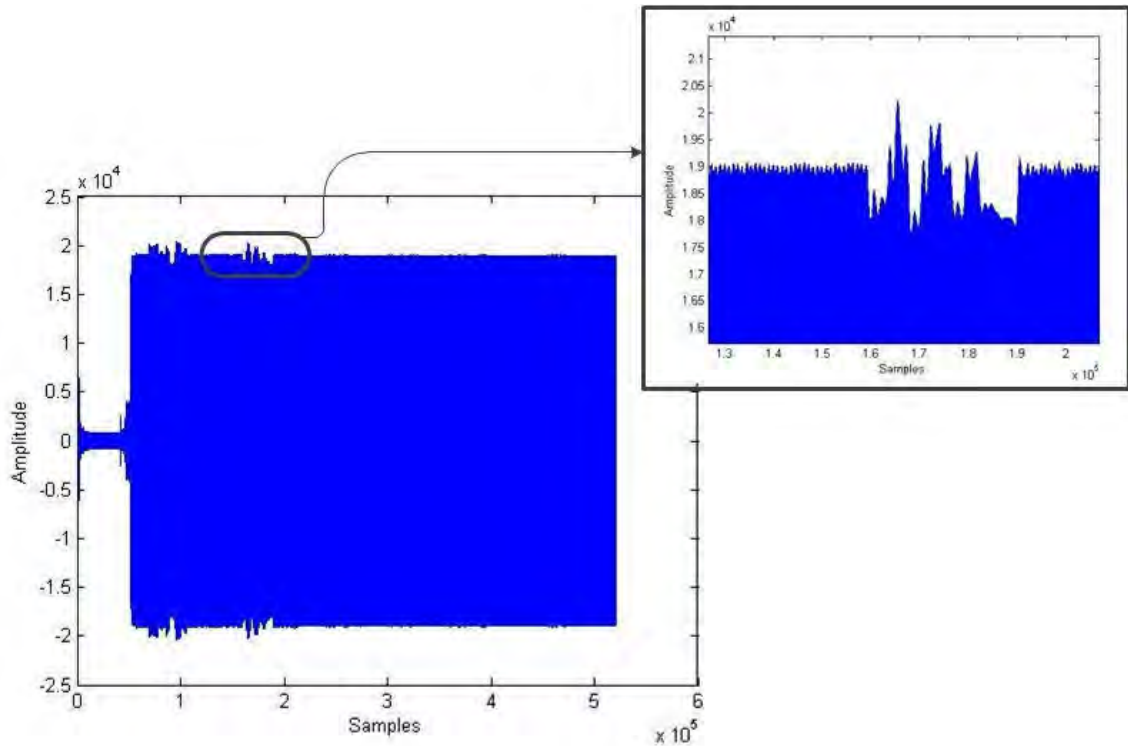


Figure 7.21: Interference Pattern Indicating Positions of Binary ‘1’

The Hilbert transform approximation is then applied to the signal resulting in the extraction of the interference pattern envelope, as shown in figure 7.22. Where the 124.2 kHz FSK ‘1’ signal is present in conjunction with the 122 kHz EMI signal, constructive or destructive interference has occurred, resulting in a noticeable peak or trough in the interference pattern envelope. When a 134.2 kHz FSK ‘0’ has been transmitted from the tag, but has been filtered out by the 120 kHz to 130 kHz bandpass filter, the interference pattern envelope remains smooth.

By applying an upper and lower threshold limit to the interference pattern envelope and monitoring the bit-timing, the bit-stream can be extracted. In this example case, when the envelope is between the thresholds a ‘0’ is demodulated, while when the envelope is outside of these threshold limits, an FSK ‘1’ signal is demodulated.

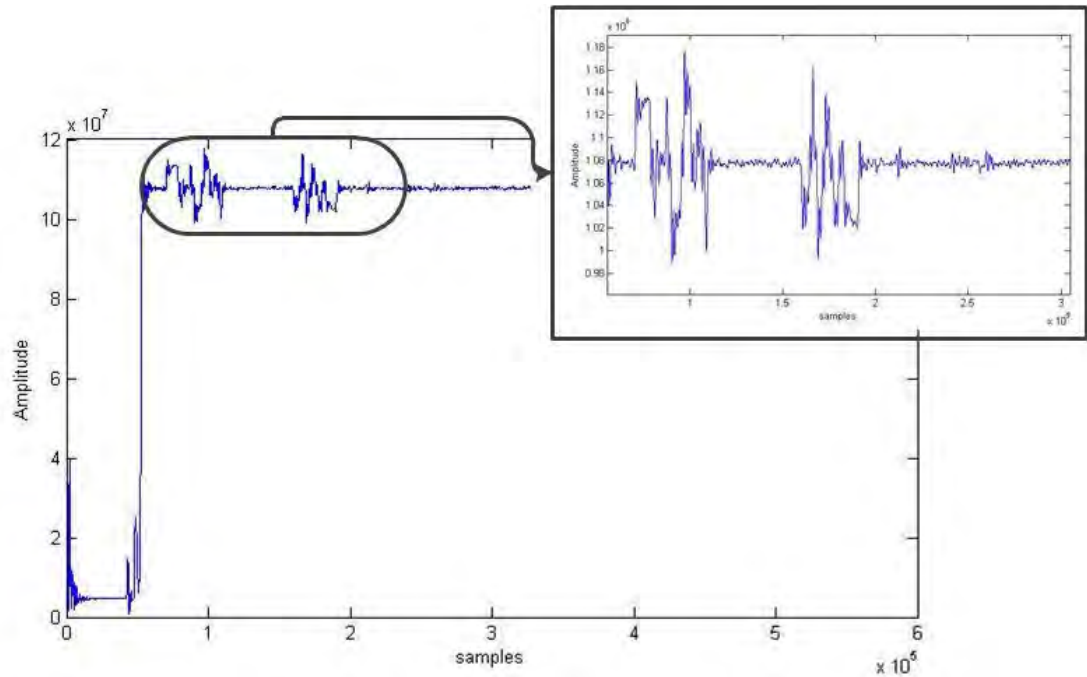


Figure 7.22: Interference Pattern Generated by Tag Signal

These threshold limits are assigned by the EMI analyser block, which monitors the EMI envelope during analysis and stores the base-band level. The threshold limits are set as a percentage above and below the EMI envelope base-band level. The magnitude of this percentage is dependent of the nature of the inherent ripple created by the IIR filter and the ripple of the envelope of the received EMI signal. When the interferer signal takes the form of a highly coherent narrowband signal, these percentage values can be set very low, in the region of 2 to 3%, while less coherent EMI signals lead to a higher degree of ripple within their base-band level.

During instances where the base-band envelope ripple is quite high, it is required that the tag signal be of suitable strength to create an interference pattern in excess of the base-band ripple to allow effective demodulation. When the tag signal is of especially low amplitude in comparison to the EMI signal, the interference pattern becomes increasingly difficult to extract from the base-band ripple to achieve effective demodulation.

The choice of the lowpass filter within the Hilbert transform approximation has to be carefully chosen to allow the effective extraction of the interference pattern. If

too low a cut-off frequency is assigned, it will affect the transience of the interference pattern envelope, while a higher cut-off frequency will not effectively remove the higher frequency carrier signal. For this application a 20 kHz signal proved effective. Care must also be taken to ensure that slow transitions of the interference pattern signal through the base-band region are not mistaken for an absence of constructive and destructive interference. This has been achieved by careful timing of the bit-positions, but errors can occur during instances of high base-band ripple and low level tag signals.

7.6 FPGA Configuration

The standard method for the configuration of Xilinx[®] FPGAs is through the use of the boundary scan method directly from the PC via a JTAG interface [13]. The Xilinx[®] Spartan 3e FPGA family are volatile CMOS-based SRAM devices which means that they cannot retain their configuration on system power-down. To alleviate the need to manually reconfigure the device on each system start-up via the JTAG interface, automatic re-configuration can be achieved from an external non-volatile memory IC. A 16 Mbit ST Microelectronics[®] M25P16 Serial Flash PROM device is provided on the Enterpoint[®] Darnaw1 module for this purpose. This device can be used in many ways in conjunction with the FPGA. It can be loaded with a single FPGA configuration, allowing automatic configuration, loaded with two FPGA configuration files, allowing the FPGA to be reconfigured automatically, it can store non-volatile data for any processes operating on the FPGA or it can store processor code to be run on a hardware microprocessor configured on the FPGA. [3]

For this system the serial flash memory device is loaded (via JTAG) with a single bit-level configuration file generated by the Xilinx[®] ISE EDA tools. On system start-up a clock signal is applied to the Flash memory and the bit configuration file is bit-shifted into the FPGA allowing the device to be fully configured.

7.7 Final Implementation and Testing

The final design, as shown in figure 8.23, was implemented on PCB with a suitable PGA style header for connection of the Enterpoint[®] Darnaw1 module and an FX-2 connector for connection of the Xilinx[®] Spartan 3e Starter Kit development board can be seen to the left of the picture.

Testing of this system was carried out using the experimental setup described in section 8.2.1. The system was initially tested in a low EMI environment with the output bit-stream validated with the CRC error detection algorithm, described in section 3.7.4. This algorithm was implemented on an external microprocessor, which emulates the operation of the Auto-ID system control board.



Figure 7.23: Final DSP FPGA Auto-ID System

Upon testing of the initial prototype device, it was found that the device could successfully interrogate animal HDX Auto-ID tags. Furthermore the device could store, in on-board RAM, the digital signal resulting from the DSP algorithm. This could then be transferred to the PC via RS232 serial connection for analysis. Read-range testing, found that range was slightly limited and further investigation into the cause of this limitation was warranted. Examination of the signals present on the signal paths found the EMI to be excessively high. This EMI was also present on the system power planes. The frequency spectrum of the observed EMI is

shown in figure 7.24. Continued investigation found that the EMI in the signal path could be traced to the high-frequency clock signals and data-lines present in the design. These findings were made based on the frequency components of the EMI matching those of the activation signal and the clock signal frequencies and their harmonics.

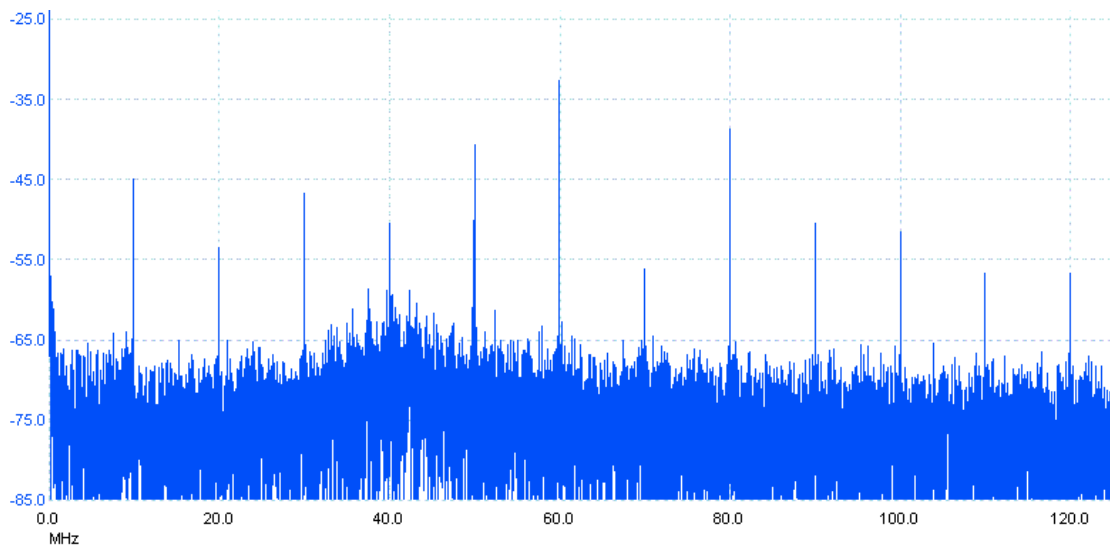


Figure 7.24: EMI Present on Analogue Signal Path during HDX Listening Period

To address the issue of self-created EMI, the PCB was redesigned as a multi-layer board, featuring split power planes and inductive and capacitive coupling of the power supply to the device and of the individual on-board ICs to the power-planes. Component placing was also revised with care taken in the physical separation of analogue (power), analogue (low-level signal) and digital devices. Opto-isolators were placed in the data lines which connect the datalines of digitally controlled analogue conditioning ICs to the FPGA control, to increase separation of the analogue conditioning circuitry from the high-speed clocking signals present within the FPGA. The revised system was retested and found to have a suitable read-range, as limited by the animal Auto-ID tag power reception and signal transmission capabilities. The final system schematic is presented in Appendix A.6.

To test the system in the presence of high levels of interference, EMI was generated by the EMI generation tool described in section 8.2.1. It was found that

the EMI analysis tool can successfully identify the spectral characteristics of the presented noise. Once the EMI present has been correctly characterised the system instantiates the appropriate DSP algorithm to allow reliable operation of the system.

EMI conditions appropriate for the instantiation of both developed DSP algorithms were created. It was found that each algorithm performed as designed. When the magnitude of the generated EMI was increased beyond those levels witnessed on-farm, it was found that both DSP algorithms for the demodulation of tag signals in the presence of EMI failed.

7.8 Results and Conclusions

This case study has described the development of an FPGA based DSP animal Auto-ID reader, capable of being deployed in an agricultural dairy environment. The resulting system has been shown to operate in real-time, successfully activating HDX animal Auto-ID tags, receiving tag response signals, applying analogue signal conditioning, digitising the signals, applying DSP algorithms to the signals and finally demodulating the signals into the animal Auto-ID codes ready to be verified with the CRC-16 error detection algorithm. The system also has the ability to capture and store in on-board RAM, 36864 samples of the digitised signal resulting from the application of the DSP algorithm to the digitised tag signals. This data capture can be later used for system refinement.

A novel DSP algorithm has been developed which has the ability to instantiate a particular demodulation scheme based on the in-system characterisation of the EMI present within the environment. In-system EMI characterisation is performed through the use of a simplified spectrum analysis tool. In the presence of low level EMI, a standard bandpass filter and frequency counting FSK demodulation routine is employed. When higher levels of EMI are detected, the system operates one of two developed demodulation algorithms dependent on the results of EMI characterisation. In the presence of a single narrowband interferer, the system ignores that FSK band where the interferer is present and performs a demodulation

routine using solely signal information from the other FSK band. If an EMI interferer is present in both FSK bands, demodulation is performed by observation of the interference pattern which is created between the interferer signal and the Auto-ID tag signal.

7.9 References

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Chapter 8

Case Study 5: Smart ID Numbering for Industrial Grade Animal Auto-ID Tags

8.1 Introduction

The amplitude of the activation signal received by the Auto-ID tag and the amplitude of the tag response signal received by the reader antenna is greatly dependent on the distance between the tag and the reader antenna, as described in section 2.2.2. Therefore, as the distance between the Auto-ID tag and the reader antenna increases, the amount of energy harvested by the tag reduces, resulting in a lower amplitude response signal being generated by the tag. In addition to this, the further away the tag is the lower the amplitude of the tag response signal received by reader with respect to that transmitted by the tag. Case Study 3 has presented an analysis of high level Electro-Magnetic Interference (EMI) present on certain dairy farms. These factors of tag distance and EMI combine to impose a limit to the read-range of the Auto-ID system. This read-range is reached when either the tag cannot harvest enough energy to activate, or the signal transmitted by the tag is of such a low level that it falls below the EMI level present at the reader antenna. As described in section 3.5.4, current animal Auto-ID tags often perform with reduced range in the presence of high EMI, where, effectively, strong tag response signals are being drowned out by elevated levels of EMI. This reduced read-range can greatly affect the operation of the automated milking parlour.

During examination of the received and demodulated tag signals, certain patterns in the Bit Error Rate (BER) were noted. This case study aimed to exploit these BER patterns to increase the probability of correctly deciphering a tag ID and maintaining read-range in the presence of high levels of EMI.

8.2 Examination of Tag Performance in High EMI Conditions

8.2.1 Experimental Setup

HDX animal Auto-ID tags take many forms, as described in section 3.5.1. The most popular form used for dairy farm automation purposes is the Texas Instruments® TIRIS circular ear tag. This tag type provides a listed read-range of up to 60cm [1], but in practice read-ranges of up to 1 m are achieved. Allflex® are the world's most widely used animal Auto-ID tag supplier and exclusively employ Texas Instruments® TIRIS type Auto-ID tags [2]. These tags are then placed in a protective housing by Allflex®, suitable for application to the animal's ear. For experimentation in this case study TIRIS ear tags will be used. The industry standard Texas Instrument® TIRIS Series 2000 RFID reader [3], coupled with the Dairymaster® calf feeder antenna, will be used to analyse the performance of animal Auto-ID tags in the presence of EMI.

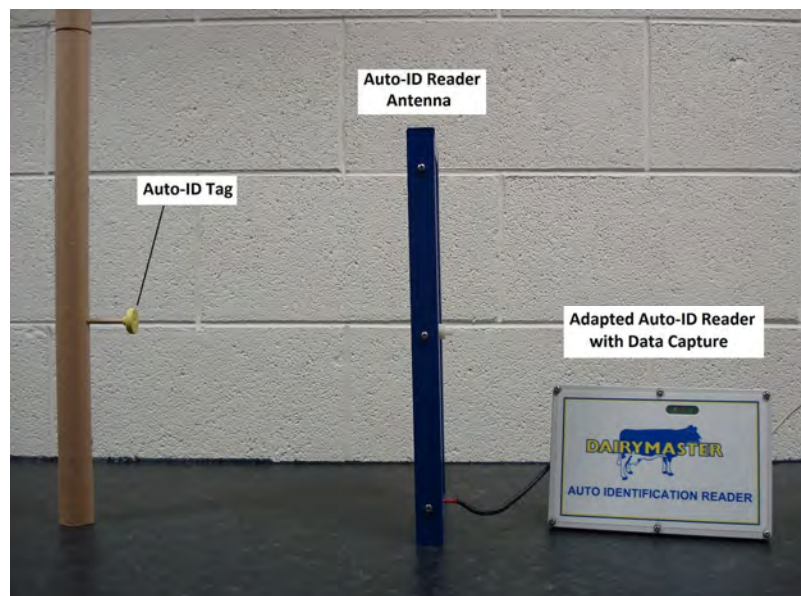


Figure 8.1: Auto-ID Tag Interrogation Testing

A series of 20 24mm circular TIRIS animal Auto-ID tags were acquired from Texas Instruments®. Each tag was mounted on a movable non-metal stand with the reader antenna and tag antenna coils parallel. The maximum range of the Auto-ID system configuration was noted as 35cm. A data capture system was connected to the data output Auto-ID reader module to allow the capture and storage of received and demodulated tag data, even when the data failed the CRC error checking routine. The

testing configuration is shown in figure 8.1. This data capture routine was implemented in Processing code, which is presented in Appendix A.8.



Figure 8.2: EMI Generation

It was noted in Chapter 6 that Low-Frequency (LF) EMI encountered on-farm can be broadly divided into two main categories; on-farm ‘bursty’ EMI and off-farm ‘continuous’ EMI. Here both of these categories of EMI were generated for use in experimentation. Suitable EMI was generated using the Keithley® 3390 Arbitrary Waveform Generator [4] and associated Keithley® KIWAVE software [5]. To allow the transmission of these EMI signals an antenna circuit and matching network were created, through the National Access Program (NAP) at The Tyndall Institute, UCC [6]. The complete EMI generation system is shown in figure 8.2.

The EMI source was introduced to the experiment perpendicular to the Auto-ID reader antenna at a distance of 3 m and the amplitude of the EMI was increased until it was similar to that received in the field and gave the desired tag ‘missed reads’. This EMI had the effect of reducing the read-range of the system to less than 20cm. The tag was moved to a distance of 22cm from the reader antenna to allow the observation of the profile of the errors within the received bit stream.

8.2.2 Tag Transmission Characteristics

The response signal from a Texas Instruments® TIRIS tag was examined by connecting a high impedance oscilloscope probe to the tag antenna terminals. The

resulting signal capture is shown in figure 8.3. It was noted during the examination of the response received from the passive animal Auto-ID tags, that as the tag transmission progressed, the amplitude of the transmitted signal diminished. More in-depth examination of the TIRIS HDX animal Auto-ID tags found that, as would be expected, the voltage present on the tags power storing reservoir capacitor was diminishing as the transmission progressed. In short, the tag was running out of stored energy, resulting in a reduction in the amplitude of the transmitted signal. During investigations, it was noted on a number of occasions that the voltage on the capacitor dropped below the operating voltage of the tag circuitry during the response transmission and the transmission ceased before the entire tag ID had been transmitted. Figure 8.3 shows the charge-up of a tags reservoir capacitor during the activation period and the diminishing amplitude of a tag transmission during the response period.

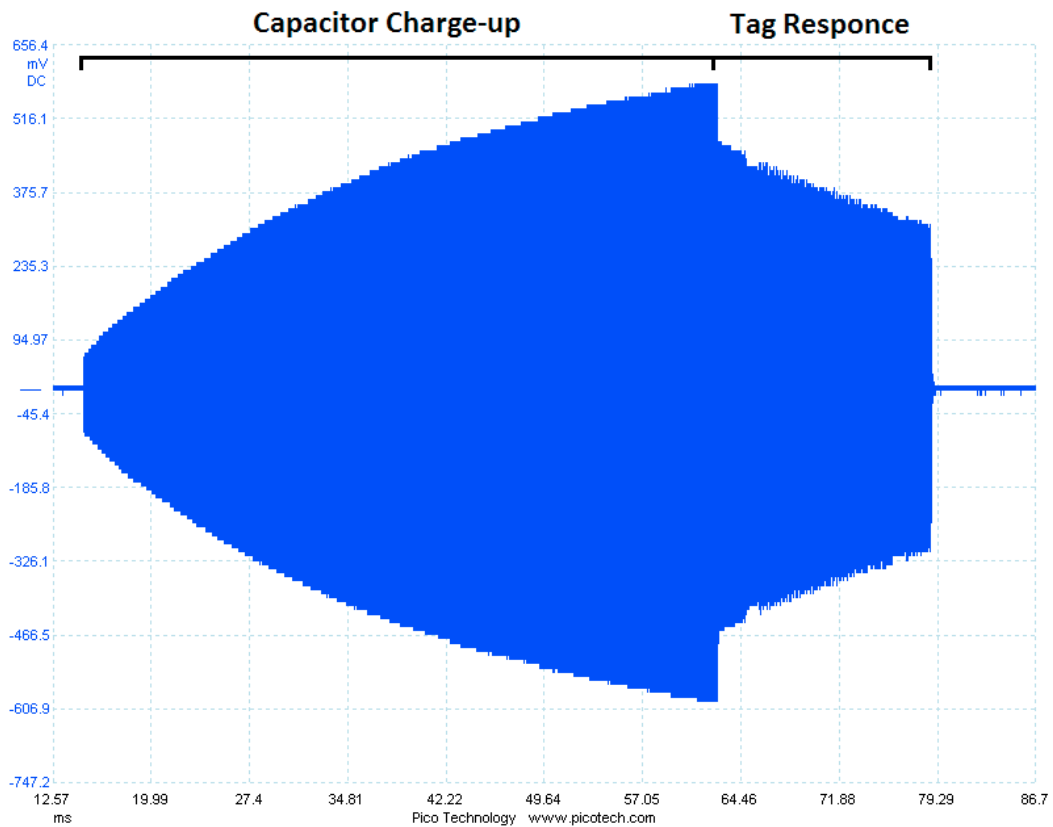


Figure 8.3: Decreasing Amplitude of Tag Response

8.2.3 Auto-ID Tag Performance in ‘Bursty’ EMI

‘Bursty’ EMI takes the form of an intermittent signal with a roughly Gaussian distribution of frequency and intensity. A series of 500 tag interrogations were performed on a single TIRIS Auto-ID tag with the resulting bit-streams logged on reception of a start of stream header. This was performed in the presence of random ‘bursty’ EMI centred on 130 kHz and with amplitude in the order of what was witness in the field, as generated by the EMI generation system. This was repeated for a total of 20 TIRIS Auto-ID tags. It was found during testing that in the presence of ‘bustly’ EMI that the BERs within the received code of an animal Auto-ID were broadly evenly distributed over the data transmission. This has the result that while the entire tag ID may never be received correctly in a single tag read, that different sections of the tag-ID were received and demodulated correctly with each successive tag read. Examination of the resulting bit-streams found that by amalgamating a number of incorrect bit streams of the same Auto-ID tag, the correct animal ID number could be constructed using the data from a number of incorrect tag reads.

8.2.4 Auto-ID Tag Performance in Continuous EMI

In the presence of ‘continuous’ type EMI the drop in amplitude described in section 8.2.2 often results in the beginning of the tag transmission being received correctly, but as the amplitude of the transmission falls, the tag signal, as received by the Auto-ID reader, drops below the EMI level and therefore becomes more difficult for the reader to demodulate the signal correctly. This results in a higher concentration of errors in the latter part of the transmission. This latter part of the transmission where errors become more prominent is the 16-bit section containing the CRC code for error detection. Therefore, in some cases, the ID code is being received correctly but errors within the error detection code are causing the ID-code received to be flagged as incorrect.

To examine the BER distribution in more detail an experiment was conducted with a series of 20 TIRIS ear-tag style animal Auto-ID tags which were interrogated in the presence of EMI, as described in section 8.2.1. It should be noted that predominantly industrially numbers TIRIS tags were used [7], with codes not

adhering to ISO animal ID numbering. Their operation is identical to those used in ISO compliant systems.

The observed decrease in transmission amplitude results in an increased BER as the transmission progresses. Therefore the first bit of the tag ID to be transmitted is much more likely to be received correctly than the final bit, or the following 16 bits which make up the CRC error detection code.

Figure 8.4 illustrates a typical BER distribution of Auto-ID tag response in Continuous EMI just beyond the tag read-range. The tag was interrogated 75 times in high level Bursty EMI conditions and the average value of each bit location was calculated. It is clear that a decision on logic '1' or '0' can be made for the early part of the bit-stream. This decision becomes almost impossible, later in the bit-stream. These results lead to the belief that advantages may be achieved by allowing animals to be identified using less digits on-farm, while still providing full 64-bit ID codes, plus CRC code, for off-farm use.

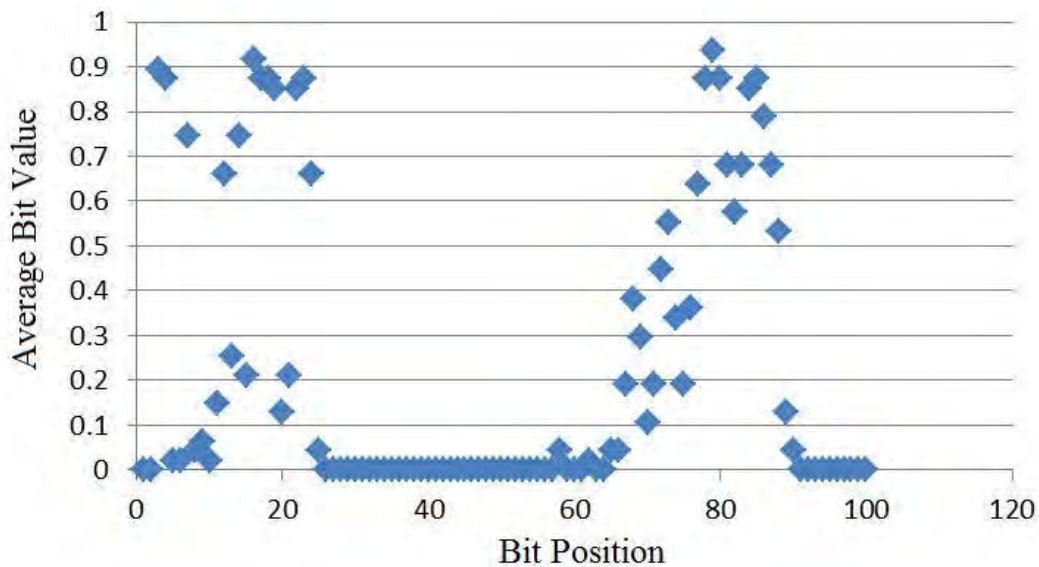


Figure 8.4: Auto-ID Tag Bit-Error Distribution

This experiment was repeated for a total of 20 TIRIS-based 24mm ear-tag style Auto-ID tags. Each tag was interrogated 75 times in the presence of narrow-band EMI of frequency 134.2 kHz, with the tag placed at a location just beyond the successful

read-range. The demodulated response generated by the Texas Instruments® TIRIS Series 2000 reader was logged for each interrogation. This data was then amalgamated into a single database with each interrogation result being compared to its known ID-code bit-stream. In the Frequency Shift Key (FSK) modulation scheme used in this technology, the reception of a 134.2 kHz EMI signal corresponds to a digital ‘0’, which will result in a number of ‘1’ bits being overcome by the EMI and resulting in the demodulation of a ‘0’. To determine the probability of correctly receiving a ‘1’ when a ‘1’ was transmitted, the contents of each bit location which should contain a ‘1’ were summed for all 75 samples, with the result divided by 75. Figure 8.5 shows the results of testing carried out on four of the twenty tags tested, with slightly elevated levels of EMI used for demonstration purposes. The BER can be seen to increase in as the transmission progresses.

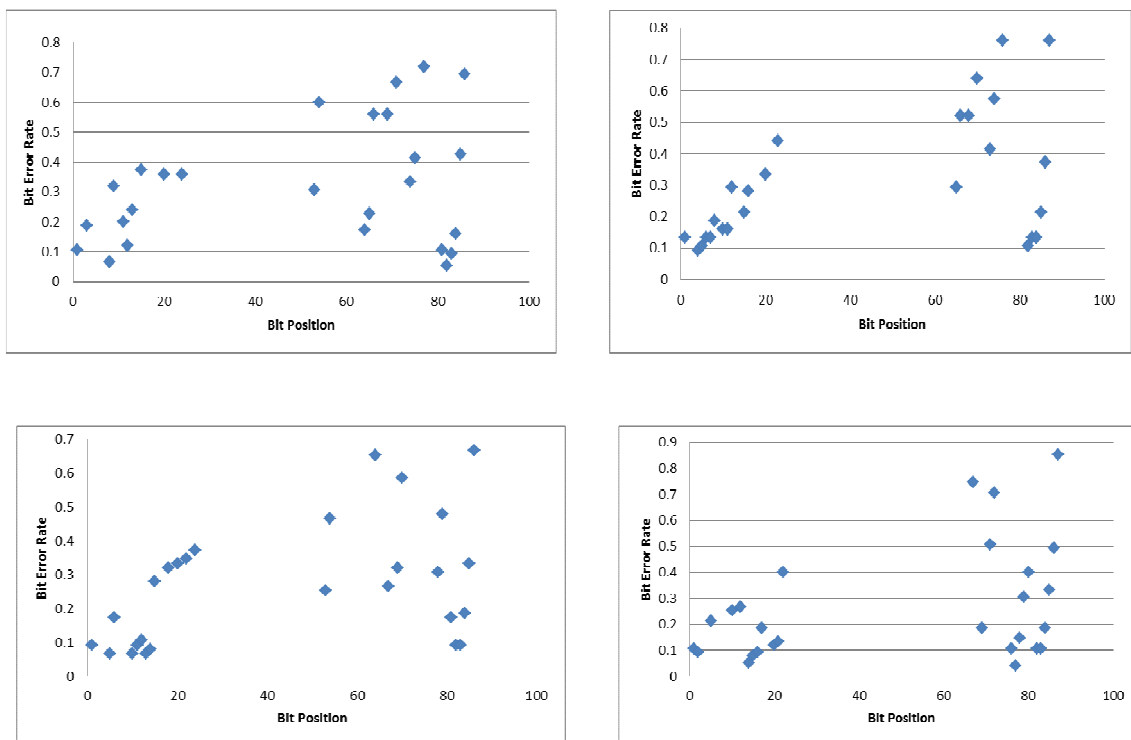


Figure 8.5: Increasing Bit Error Probability Vs. Bit-Location

8.3 Multi-Read Averaging in ‘Bursty’ EMI Conditions

8.3.1 System Hypothesis and Development

In ‘bursty’ type EMI it has been shown that the bit-errors are relatively evenly distributed throughout the bit-stream and it may be possible to discern the correct tag ID number from an amalgamation of the various incorrect tag bit-streams. Where the bit-stream demodulated from the tag signal is constantly present (as indicated by the tag bit-stream start block) but is repeatedly failing the CRC, the bit-streams of all failed reads which can be reliably labelled as being from a single tag (based on a specific time-window) are compared. For example, if 10 reads are made in 0.7 s and each fails, each fail may be due to a single bit errors but in a different location in the bit-stream due to random ‘bursty’ noise.

An animal Auto-ID reader control and data capture system was developed which would monitor the bit-stream received by the reader module in order to recognise any tag header sequence of ‘01111110’ and then capture the following 80-bit (64-bit ID and 16-bit CRC) bit-stream and performs the standard CRC-16 check to ensure correct reception and demodulation.

If the 64-bit ID code fails the CRC-16 error detection routine, the 80-bit bit-stream is stored in an on-board memory location and another tag interrogation is requested. The process is then repeated until either the ID code passes the CRC error detection routine or a series of 10 bit-stream samples have been collected.

At this point an averaging algorithm is executed to determine a decision and confidence value to associate with each bit-location in the bit-stream. The bits of each bit location (1 to 80) of all 10 samples are summed and then, based on the result, a confidence percentage is generated. This percentage is the number of times the binary code (‘1’ or ‘0’) is received in that location divided by the total number of samples, with the result multiplied 100%.

By now employing a suitable confidence threshold, a decision on the true value of the bit in each bit-location can be made. Experimentation found that a confidence

threshold of 75% often produced favourable results, but the threshold is dependent on the EMI intensity in a given location. Once this decision process is complete, an additional cross-referencing check can be made with the farm automation herd management software database of known correct animal tag ID numbers present on farm. The multi-read averaging algorithm was implemented in Processing code, which is presented in Appendix A.9.

8.3.2 System Evaluation

To evaluate the developed system an experimental layout as described in section 8.2.1 was arranged, with ‘bursty’ type EMI being transmitted from the EMI generator. Ten reads of each single tag with known ID numbers were performed in bursty EMI conditions. This resulted in each tag read failing the CRC error detection routine. On each attempted read, once the HDX start block was detected, the following 80-bits (64 ID and 16 CRC) were logged. An example of the first 16 bits received after each successful tag header read is shown in table 8.1, with any bit which was detected in error highlighted in yellow.

Sample	Header								Bit Location															
									1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1	0	1	1	1	1	1	1	0	0	0	0	1	0	0	1	0	0	0	1	0	1	1	1	1
2	0	1	1	1	1	1	1	0	0	0	0	1	0	1	0	1	0	0	0	0	0	0	1	1
3	0	1	1	1	1	1	1	0	0	0	0	1	0	1	0	1	0	0	0	1	0	0	1	0
4	0	1	1	1	1	1	1	0	0	0	0	1	0	1	0	1	1	0	0	1	0	0	1	1
5	0	1	1	1	1	1	1	0	0	0	0	1	0	1	0	1	0	1	0	1	0	0	1	1
6	0	1	1	1	1	1	1	0	0	0	0	1	0	1	0	1	0	0	0	1	0	1	1	1
7	0	1	1	1	1	1	1	0	0	1	0	0	0	1	0	1	0	0	0	1	0	0	1	1
8	0	1	1	1	1	1	1	0	0	0	0	1	0	1	0	0	0	0	1	0	0	0	1	1
9	0	1	1	1	1	1	1	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	1	1
10	0	1	1	1	1	1	1	0	1	0	0	1	0	1	0	1	0	0	0	1	0	0	1	1

Table 8.1: Summary of Data Capture to Determine BER

According to the developed algorithm, as none of the captured bit-streams passed the CRC-16 error detection algorithm, the resulting data were processed as described above and resulted in a series of predictions and confidence percentages, as shown in table 8.2.

Bit Location	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Decision	0	0	0	1	0	1	0	1	0	0	0	1	0	0	1	1
Confidence (%)	90	90	100	80	100	90	100	90	90	90	100	90	100	80	100	90

Table: 8.2: Bit Location Prediction and Confidence Value

By implementing a simple confidence threshold of 75% the known true bit-stream of “0001010100010011” was extracted. This proved true for the entire 80-bit stream of all 20 tags tested in the presence of low intensity EMI which had led to a 0% read-rate before multi-read averaging had been applied. It was found that as the intensity of the bursty EMI was increased, the achieved 100% read-rate dropped, due to the increased frequency of errors in the demodulated bit-streams.

8.4 Development of a Novel Smart ID Numbering Protocol

8.4.1 System Hypothesis

As described in section 8.2.4, in the presence of ‘continuous’ type EMI, the probability of bit error increases as the transmission continues, with the result that the CRC-16 error detection block is the section of the received tag ID which has the highest probability of containing bit-errors or, on occasion, is not transmitted due to insufficient power available to the tag.

Therefore, in some cases, the animal ID bit stream is received correctly but errors in the error detection code cause the ID received to be flagged as incorrect. To counteract this, it is envisaged that if an error detection code is inserted earlier in the ID transmission, within the 64-bit ID code, improvements in tag performance can be achieved. As the format of ID numbering for animal Auto-ID for traceability purposes is governed by ISO standardisation, it is expected that this system will be used only for on-farm automation purposes.

8.4.2 Current Animal Auto-ID Tag Numbering

ISO 11784:1996 standardises the animal ID-numbers to be stored on animal Auto-ID tags, but, in practise, the ID information stored on an animal Auto-ID tag applied

to a dairy animal is not always in compliance with this standard. It often takes the form of the Texas Instruments[®] industrial tag standard, which consists of the 12-bit application code and a 52-Bit ID-code [7]. There are various reasons why ISO coding is not used, the most common being administration costs involved in assigning ISO standardised Auto-ID tags to each animal.

Also, in practice, all 52-Bits of the industrial ID code are not used for animal ID. As these tags are not ISO compliant, a world-wide unique identifier for animal traceability purposes is not necessary. For the purpose of farm automation, it is only required that each Auto-ID tag number is unique within each facility. Therefore many systems, including that of this project's industrial partner, use only the 8 least significant decimal digits of the ID code for unique animal identification on farm. This allows for a more than adequate 99999999 uniquely identifiable animals in each facility. Such a number can be represented with 28 binary data bits, leaving 24 superfluous bits within the tag ID. These are often set to zero.

8.4.3 Industry Led Tag Numbering Guidelines

As this numbering system has been developed for compatibility with the existing Dairymaster[®] animal Auto-ID system, certain guidelines have to be followed to allow back-compatibility with existing installed equipment. Through consultation with Dairymaster[®] personnel it was found that a 16 digit ID number, preceded by three HEX digits representing an application code, would be desirable for operation with their current herd management system. Dairymaster[®] herd management software uses only the 8 least significant digits of an animal ID code to discriminate between animals on-farm. The system uses the animal flag bit (see section 3.6) to determine whether the tag is an ISO compliant animal tag or an industrially coded tag. This flag bit is located at the most significant bit (MSB) of the animal ID-code.

8.4.4 Advanced ID Number Generation

The required 8 decimal digit ID numbers are generated from the first 26-bits of the binary ID code. The use of 26-bits allows for, a more than adequate, decimal ID number range of '00000000' to '67108864' for on-farm animal identification. To

allow for operator usability in manual data entry, this will be preceded by four decimal zeros, which in turn is preceded by the 4 digit error checking code.

To generate the 4 digit CRC, a 12-bit CRC code is used. This is reduced capacity CRC is deemed sufficient as, while the CRC-16 of the standard ID number provides error checking for all 64-bits, this CRC-12 is only checking 26-bits pertaining to the 8 digit animal identifier. The CRC-12 used here is based on the 3rd Generation Partnership Project (3gpp) [8] standard for telecoms which uses CRC polynomial 0x80F. The result of this operation is a 12-bit binary CRC code which is converted to a 4-digit decimal number within the range 0 to 4095.

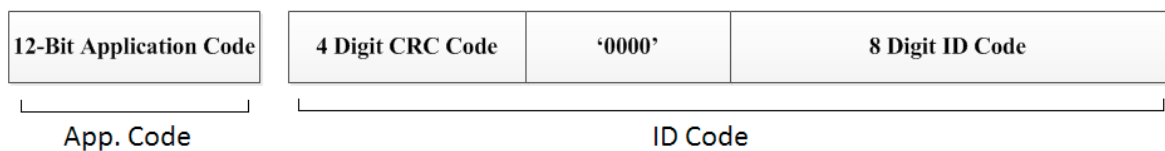


Figure 8.6: Advanced ID Number Composition

The resulting 16 digit number is then converted to a 52-bit binary number. If the number can be expressed with less than 52-bits it is zero-padded in the most significant bit locations to become 52-bit. The 11 least significant bits (LSBs) of the 52-bit ID number are then XORed with an 11-bit binary number ‘10010110101’ and the result is used as the bits 2 to 12 of the Application Code, while the animal flag (bit 1) is set to ‘0’. This gives an additional error checking which allows the verification of the 11 LSBs. Even though these eleven LSBs are not guaranteed to be unique within the ID numbers present in the dairy facility, they can be cross referenced with the ID numbers present in the herd management system to allow a confidence-based identification of the animal.

The result is the ID format shown in figure 8.6. A flow diagram of the ID number generation is shown in figure 8.7, with an example of a generated ID given in table 8.3. The MATLAB[®] script for the generation of these ID numbers is presented in Appendix A.10.

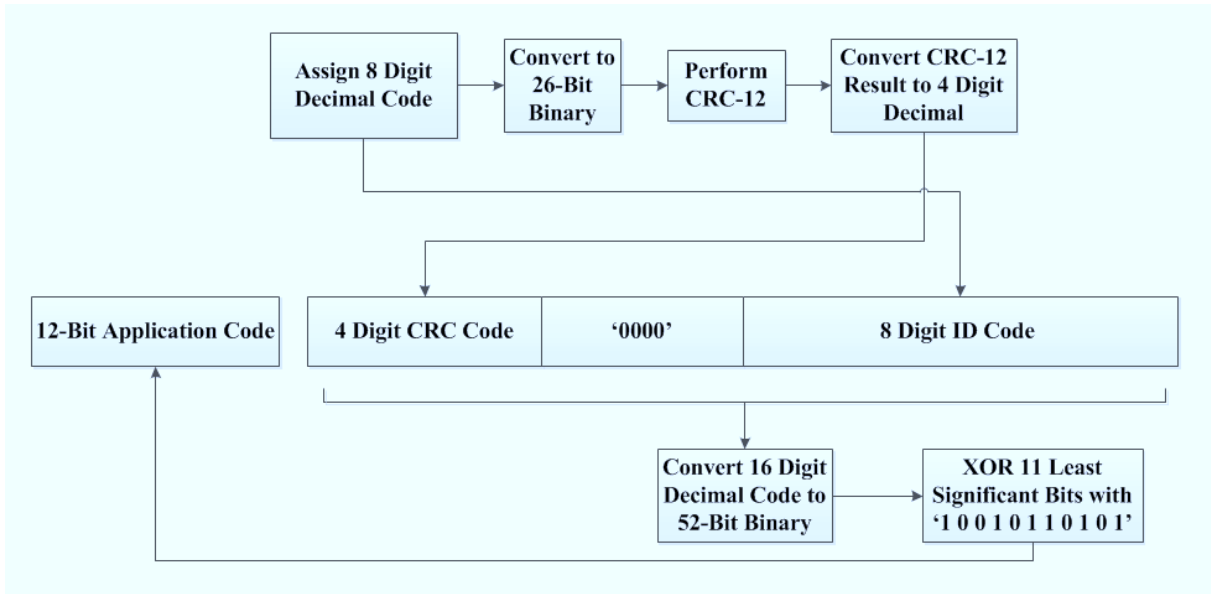


Figure 8.7: Creation of Advanced ID Code

Random 8-digit Animal Identifier (Decimal):	14772186
8-digit Animal Identifier (26-Bit Binary):	111000010110011000000000
CRC-12 of Animal Identifier (12- Bit Binary):	1100011000
CRC-12 of Animal Identifier (Decimal):	792
Decimal Tag number:	792000014772186
Tag Number (52-Bit Binary):	10110100000101000000000000 000000000000000000000000
Application Code (12-Bit Binary):	1101101111
Application Code (Hex):	36F

Table 8.3: Example ID Code Generation

To complete the tag ID, the CRC-16 routine is carried out on the entire 64-bits of data, to generate a 16-bit error detection code to be appended to the end of the transmission

8.4.5 Advanced ID Decoder and Error Check Routine

As these tags conform to the Texas Instruments[®] industrial tag formats, they are designed to be readable by any animal auto-ID reader which can interrogate TIRIS and ISO based animal Auto-ID tags. A Smart animal Auto-ID reader control system has been developed to enable the additional error checking features built into the ID number of the tag.

On initial reception, the 64-bit ID number is checked using the standard CRC-16 algorithm. Only if this error check fails, are the extra error checking features used. Firstly the 64-bit ID number is divided into a 12-bit application code and a 52-bit ID-code. The 52-bit binary ID code is then converted into a 16 digit decimal number. The 8 least significant digits of this decimal number represent the animal ID used in the DM herd management software. This number is checked using a CRC-12 error check, using the 4 most significant digits.

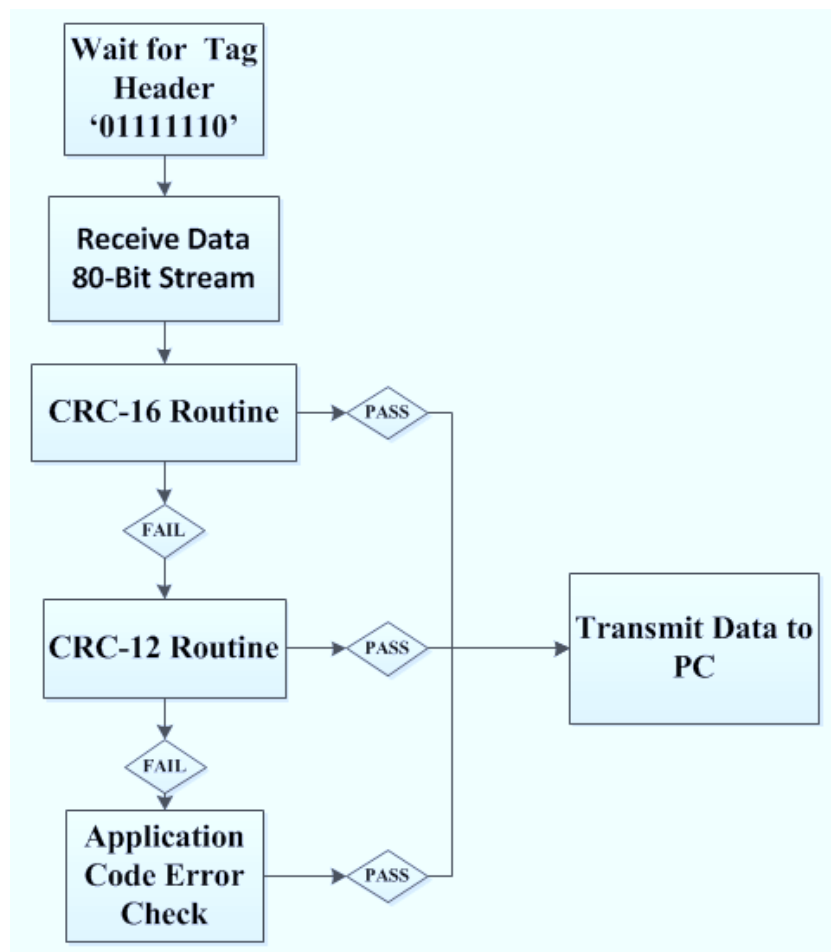


Figure 8.8: Tag Error Check Procedure

If this CRC-12 error check passes, then the 8-digit ID number is said to be correct and is passed to the herd management software. If it fails the next error detection method is called. The 11 least significant bits of the 52-bit ID number are XORed with 0b01101101111. The result is compared with the 12-bit application code, noting that the MSB is reserved as an animal flag. If this error detection passes, it can be

assumed that the first 11-bits of the transmission are correct, and the error which caused the CRC-12 to fail is outside of these bits. This 11-bits string is then transmitted to the PC where it can be cross-checked against the animal IDs present in the farms herd management system in the hope of finding a unique match. A flow diagram of this process is shown in figure 8.8. The MATLAB[®] script used to perform this error checking routine is presented in Appendix A.11.

8.4.6 Development of an Animal Auto-ID Tag Simulator

To test the developed numbering and additional error checking system, a number of Animal Auto-ID tag vendors were approached to manufacture custom Auto-ID tags which would be pre-programmed with ID-numbers created using the algorithm. It was found that the custom programming of a suitable number of tags for experimentation purposes was beyond the financial limitations of this project. Therefore, a tag simulation system was developed.

The ear-tag style HDX animal Auto-ID tags consists of a control IC with embedded EEPROM, a reservoir capacitor and an antenna circuit consisting of a coil of 24mm in diameter made from extremely narrow gauge wire, with an inductance of 2.5mH and a resistance of 34 Ω , and a 555 pF capacitor. The combination of this inductive antenna and the given capacitance gives the antenna circuit a resonant frequency of 134.2 kHz. [1]



Figure 8.9: (Left) TIRIS Circular Auto-ID Tag [1] and (Right) Allflex[®] HDX Animal Auto-ID Ear-Tag [2]

The antenna circuit of the HDX animal Auto-ID tag simulator was constructed from a tightly wound narrow-gauge loop antenna, identical to that used in Texas Instruments[®] TIRIS tags. The loop antenna was tuned to resonance at 130 kHz with a 550 pF capacitor with a 0 – 40pF variable capacitor in parallel. The antenna was damped with a parallel resistance of 33k Ω to provide greater control over the antenna signal. Two contact points were inserted into the circuit to allow the connection of the output from a signal generator.

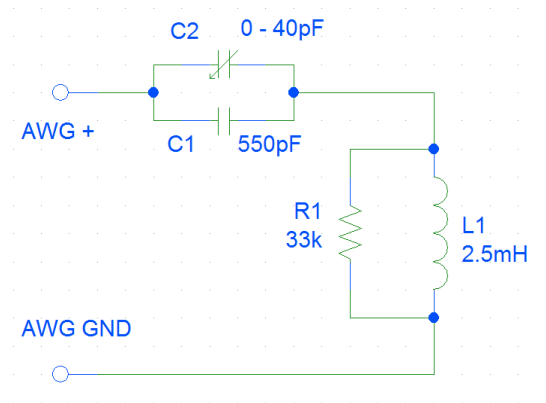


Figure 8.10: Tag Simulator Antenna Circuit

Five advanced animal ID numbers were created using the algorithm described in section 8.4.4. Based on these animal IDs, a series of 5 animal Auto-ID tag response signals were designed using the Keithley[®] KIWAVE waveform generation tool [5]. The signal was developed using the FSK modulation scheme outlined in section 2.2.3, with the additional feature of descending amplitude as the transmission progressed, as shown in figure 8.11. These waveforms were then downloaded to the Keithley[®] 3390 Arbitrary Waveform Generator [4].

8.4.7 System Evaluation and Results

The experimental set up outlined in section 8.2.1 and 8.2.4 was repeated with the simulation animal Auto-ID tag transmitting the generated advanced animal ID numbering signal from the AWG. The EMI generation system was configured to create a single continuous interferer signal within the frequency spectrum 120 – 140 kHz.

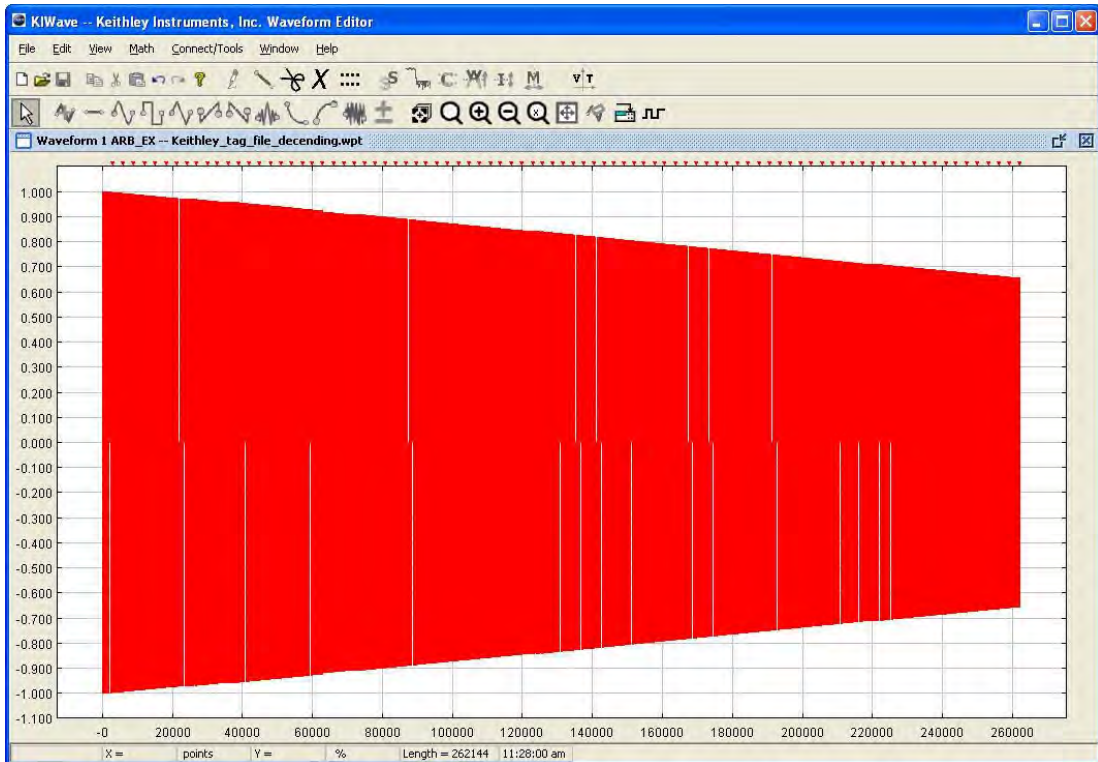


Figure 8.11: Keithley® KIWAVE GUI with Descending Tag Signal

On inspection it was found that the BER was of an identical pattern to that witnessed in testing with the established animal Auto-ID tags. As expected, this resulted in none of the received tag bit-streams passing the CRC-16 error detection routine. When the advanced ID decoding and error checking algorithm was employed, a number of the tag reads could be verified by the CRC-12 error checking routine, indicating the received bit-error was present in either the CRC-16 code or the application code. This percentage varied greatly with the intensity of the EMI signal, with almost 100% read-rate for low-level EMI, with read-rate decreasing steadily as the magnitude of the EMI increased.

The final error checking stage, the XOR of the 11 LSBs with the application code, resulted in further successful tag verification. Again, the success of the algorithm reduced steadily as the intensity of the intensity of the EMI signal was increased.

8.5 Conclusion

This case study has presented the results of an investigation into the performance of animal Auto-ID tags in the presence of varying types of EMI. Firstly the effects of ‘bursty’ type EMI was examined and found to lead to a random distribution of bit errors within a received tag signal. Secondly the effects of ‘continuous’ type EMI were examined and an increase in the BER was noted as the transmission progressed.

Based on the observed BER patterns, two novel schemes which will aid in the correct reception of animal Auto-ID information in the presence of high levels of EMI were developed and tested. By exploiting these error patterns, it was envisaged what a higher system reliability could be achieved. To account for the random distribution of bit errors in the presence of ‘Bursty’ EMI, a multi-read averaging algorithm was developed. This was tested in simulated EMI conditions and found to operate as designed.

Secondly an advanced on-farm animal ID numbering scheme was developed and tested, which allows additional error checking to occur, in conjunction with a suitably configured reader system, when operating in the presence of ‘continuous’ type EMI. This removed the reliance of the CRC-16 error check, which has been found to be contained in the area of the tag transmission statistically more likely to be received in error, leading to an increased rate of successful tag interrogation.

Both of these developed algorithms lead to a scenario where a certain confidence rating can be attached to individual sections of the demodulated tag bit-stream, as opposed to a CRC-checked confirmation of the entire ID number. Such a system can be useful in identifying an animal in instances of high EMI when the correct reading of the entire tag ID number is unlikely. In this case, a search can be implemented with the herd management algorithm, which matches the high-confidence bits of the ID number to known ID numbers present in the herd. In this way a call can be made on which animal tag has been read. Where conflicts occur, with a number of likely ID number matches additional investigations can be made based on comparisons of the confidence values achieved for each bit of the ID number. Advanced genetic

algorithms may also be developed to recover missing bits, similar to previous work carried out in damaged barcode IDs [9].

8.6 References

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Chapter 9

Conclusions and Further Research

9.1 Introduction

The work contained in this thesis has described an examination into the current state-of-the-art in animal Auto-ID systems in an agricultural setting and an identification of techniques which will yield a greater level of interrogation reliability for these systems, concentrating on the dairy sector. Extensive work has been carried out in an effort to observe and mitigate the effects which electromagnetic interference (EMI) has on the operation of animal Auto-ID systems, to allow the more efficient operation of automated milking parlours.

It was found that the presence of increased levels of EMI have a detrimental effect on the operation of animal Auto-ID systems, which is stifling the automation of many dairy parlour facilities. The end product has been a number of advancements in the area of Animal Auto-ID systems. The culmination of these efforts resulted in the development of a novel re-configurable hardware system capable of implementing advanced digital signal processing (DSP) algorithms to allow for the removal and mitigation of EMI within the Auto-ID tag signal. In addition to this, certain patterns present in the Auto-ID interrogation errors have been identified and exploited to aid in the identification of animal in high EMI conditions.

9.2 Major Contributions

The major contributions of this thesis are summarised in the following sub-sections:

9.2.1 Reconfigurable Animal Auto-ID Platform suitable for DSP

Implementation and Novel DSP Algorithm

An FPGA based animal Auto-ID reader has been developed suitable for the implementation of advanced DSP algorithms. The developed system features an in-system EMI analysis tool, which characterises the EMI present on-farm. Based on this

characterisation, and taking advantage of the re-configurability of FPGA technology, a suitable hardware DSP algorithm is instantiated within the system. The basic system, which operates in low EMI conditions, uses an extremely efficient IIR filter with a passband of 120 kHz to 140 kHz to removing all spectral components of the signal but those within the narrow frequency band containing the animal Auto-ID information. During instances where high levels EMI are present within the Auto-ID systems frequency band, a novel DSP algorithm has been developed which mitigates the effect of the EMI, allowing more reliable Auto-ID tag interrogations. If a single narrowband EMI signal is present with the frequency band of interest, it will often occupy only a single Frequency Shift Key (FSK) band, the FSK '1' frequency band (120 – 130 kHz) or the FSK '0' frequency band (130 – 140 kHz). An algorithm has been developed which allows the frequency band in which the EMI is present to be ignored, with signal demodulation being performed based solely of the information contained within the other.

During instances where both FSK frequency bands are occupied by EMI, a novel interference pattern based FSK demodulation algorithm has been developed. This algorithm observes the existing EMI signal, present before tag interrogation begins and performs a demodulation routine by monitoring the interference pattern created by the Auto-ID tag signal when combined with the existing EMI signal.

9.2.2 Animal Auto-ID Tag Performance and Bit Error Characterisation and Exploitation

Attention then turned to the animal Auto-ID tags themselves and the pattern of the bit errors present when the tag is interrogated in the presence of high levels of EMI. During investigations it was found that two distinct bit error patterns emerged. Firstly in the presence of 'bursty' type EMI, the Bit Error Rate (BER) was almost uniform throughout the tag transmission. It was found that by interrogating the tag a number of times, while the reader may not receive an error free response during a single interrogation, the resulting incorrect bit-streams may be amalgamated to form a correct bit-stream.

Secondly, in the presence of 'continuous' EMI it was found that the BER increased as the tag transmission progresses, resulting in a higher probability of bit

error for bits towards the end of the transmission. As the CRC-16 error detection number is the final block to be transmitted, it is statistically more likely to contain errors. To exploit this bit error pattern, a new animal Auto-ID numbering scheme, for use in on-farm animal identification, was developed which places additional error checking routines earlier in the transmission, resulting in an increased rate of successful tag interrogations.

9.2.3 Low Frequency Electromagnetic Interference Analysis

Case Study 3 details the development of a tool suitable for the capture and analysis of the Low Frequency (LF) EMI present on a dairy farm, which has the potential to effect the operation of an animal Auto-ID system. Through the use of suitable antenna circuitry, a data capture device and spectral analysis software, a system has been developed to evaluate EMI present on-farm. Through the examination of the resulting captured signals, the EMI present was characterised allowing the development of novel DSP algorithms to increase the potential for accurate animal identification. This EMI analysis tool also facilitates the industrial requirement for an LF EMI site-survey prior to and during the installation of animal Auto-ID systems. This allows correct budgeting for the installation process and also aids the installation process through the ability to identify and locate EMI sources in the field. To date, this device has been used by Dairymaster[®] in the field for the identification and diagnosis of EMI issues in problem installations. The system has also been demonstrated to Dairymaster[®] sales representatives in an effort to encourage them to use the system to perform on-site LF EMI surveys prior to installation (and preferably prior to budgeting) of an animal Auto-ID enabled parlour. The use of such a system in the field by Dairymaster[®] personnel will allow the creation of a large database of EMI on a worldwide scale. Further characterisation of EMI will aid in the refining of advanced DSP algorithms for the mitigation of EMI effects.

9.2.4 Other Contributions

During consultation with this project's industrial partner, a need for a low-cost Auto-ID reader module which would operate with the current Dairymaster[®] Auto-ID control board was identified. In areas where EMI, or some other factor, inhibits the range of an Auto-ID reader it is often beneficial to employ an increased number of readers in strategic locations to ensure correct animal identification. An increased

number of Auto-ID readers on site will also allow greater levels of farm automation, but the implementation of such a multi-reader system is often curtailed due to financial issues which could be alleviated by the availability of a low-cost reader module. The development of a low-cost animal Auto-ID reader module has been completed and is described in Case Study 2.

The detuning, and subsequent requirement for retuning, of LF coil-based antenna circuits is a major issue for the suppliers of animal auto-ID systems. Therefore, the development of an automated method for antenna circuit tuning is of major benefit to industry. As this is currently a manual operation, this operation requires a visit to the facility by a technician as the Auto-ID system is not a user serviceable device. Case Study 1 has described the development of a fully automated system for the tuning of the antenna circuit of an Auto-ID system, with a fully functioning prototype produced. The designed system has now been integrated into the Dairymaster[®] Auto-ID control board and has been successfully deployed in many installations.

In the early stages of the development of the automated antenna tuning device it became apparent the current method for controlling the read-range of an Auto-ID system was far from ideal. This led to the development of a low-cost digitally controlled power supply which could be used to control the magnitude of the tag activation signal generated by the animal Auto-ID reader and thereby control the systems read-range, while allowing maximum reception of tag signals through a fully tuned antenna circuit, leading to more reliable tag interrogation. This power supply can be controlled from the I/O port of a microcontroller, allowing the Auto-ID control board to control the strength of the reader modules activation field within an automated read-range adjustment algorithm. The development of this system is also described in Case Study 1.

For testing of the ID numbering algorithm with additional error checking routines, an Animal Auto-ID Tag simulator and an EMI simulator were developed. This EMI simulator was also used for the development and testing of advanced DSP algorithms described in Case Study 4. The EMI simulator allows the recreation of EMI encountered in the field and captured using the developed EMI analysis tool, to be 'replayed' in a laboratory setting. These devices can be used as a platform for the

testing of animal Auto-ID numbering algorithms and readers in the future by the simulation of real-world EMI and Auto-ID tags in a laboratory environment.

9.3: Further Work

The systems implemented here have demonstrated the benefit of the application of advanced animal Auto-ID systems. As this project was undertaken in conjunction with an industrial partner, the final outcomes had to take into account the final cost of device production. This set a limitation on the hardware costs, which had a great effect on the choice of PLD used within the system developed in Case Study 4. Therefore the DSP algorithms implemented were often curtailed due to the limitations of the PLD. One feature which shows great potential is the development of an automated EMI cancellation routine, similar to that used in commonly available devices such as noise-cancelling headphones. By accurately characterising and reproducing complex EMI signals and then subtracting the generated EMI from the received signal, it should be possible accurately remove EMI signals from the Auto-ID tag signal.

Further investigations are also warranted into the EMI patterns present in, as yet un-tested, dairy farm installations worldwide. It is envisaged through the use of the developed LF EMI analysis tool by Dairymaster[®] personnel and representatives, that a considerable database of EMI samples will be created. Through analysis of this database a greater understanding of the characteristics of LF EMI worldwide can be achieved, leading to a more informed design and installation of dairy farm systems. Further work in the development of an online or cloud-based database of worldwide EMI samples may also be proposed. Such a system, with additional location data associated with each EMI sample, would yield a worldwide EMI reference which would prove to be an invaluable resource for the effective planning and installation of LF auto-ID systems.

Further work is also required into the adaptation of the reconfigurable animal Auto-ID reader, developed in Case Study 4, for the interrogation of Full Duplex (FDX) animal Auto-ID tags. This reader has been designed with the necessary

hardware to allow the platform to be reconfigured for the implementation of advanced DSP algorithms for the interrogation of FDX tags. Further investigation will need to be undertaken, involving the characterisation of how FDX tags are affected by different EMI types, to allow the development of these advanced DSP techniques.

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Appendix A

Appendix A is contained on the Compact Disc which accompanies this thesis. It contains all VHDL and software code written during the completion of this project, along with a number of schematics of the electronic circuit which have been designed. The contents of this compact disk are listed as follows:

- A.1 Auto-Tuner Schematic
- A.2 Auto-Tuner C-code
- A.3 Digital Voltage Supply Schematic
- A.4 Digital Voltage Supply Processing Code
- A.5 Low-Cost Animal Auto-ID Module Schematic
- A.6 Low-Cost Animal Auto-ID Module Bill of Materials
- A.7 FPGA-Based Reconfigurable Animal Auto-ID Reader Schematic
- A.8 FPGA-Based Reconfigurable Animal Auto-ID Reader VHDL Code
- A.8 Bit-Stream Capture Processing Code
- A.9 Multi-Read Averaging Processing Code
- A.11 Advanced Animal ID Code Generation (MATLAB[®] Function)
- A.12 Advanced Animal ID Code Error Check (MATLAB[®] Function)
- A.13 PC-Based Animal Auto-ID Reader (MATLAB[®] Function)
- A.14 Thesis (pdf)

Appendix B

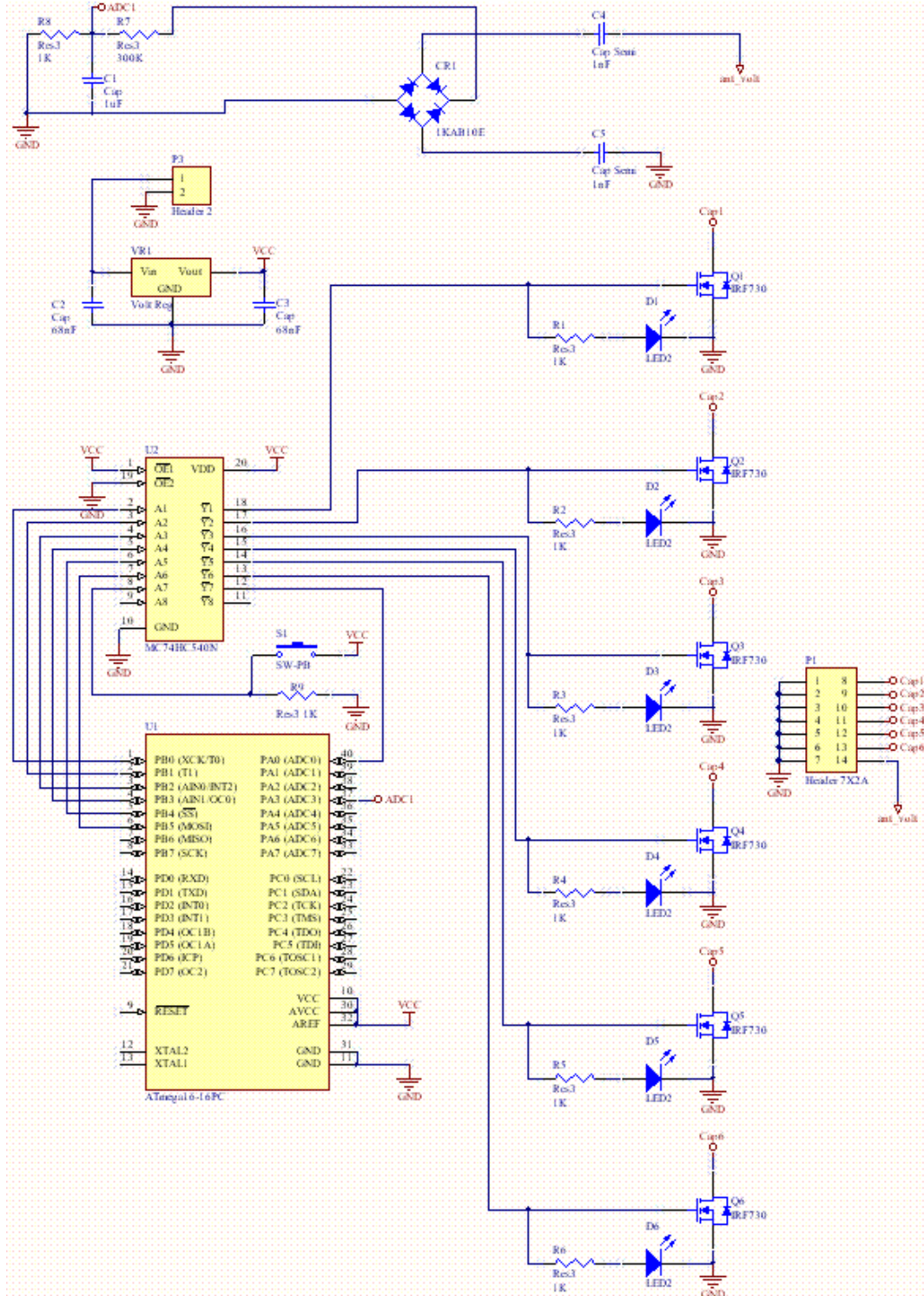


Figure B.1: Auto-Tuner Circuit Schematic (Also see Appendix A.1)

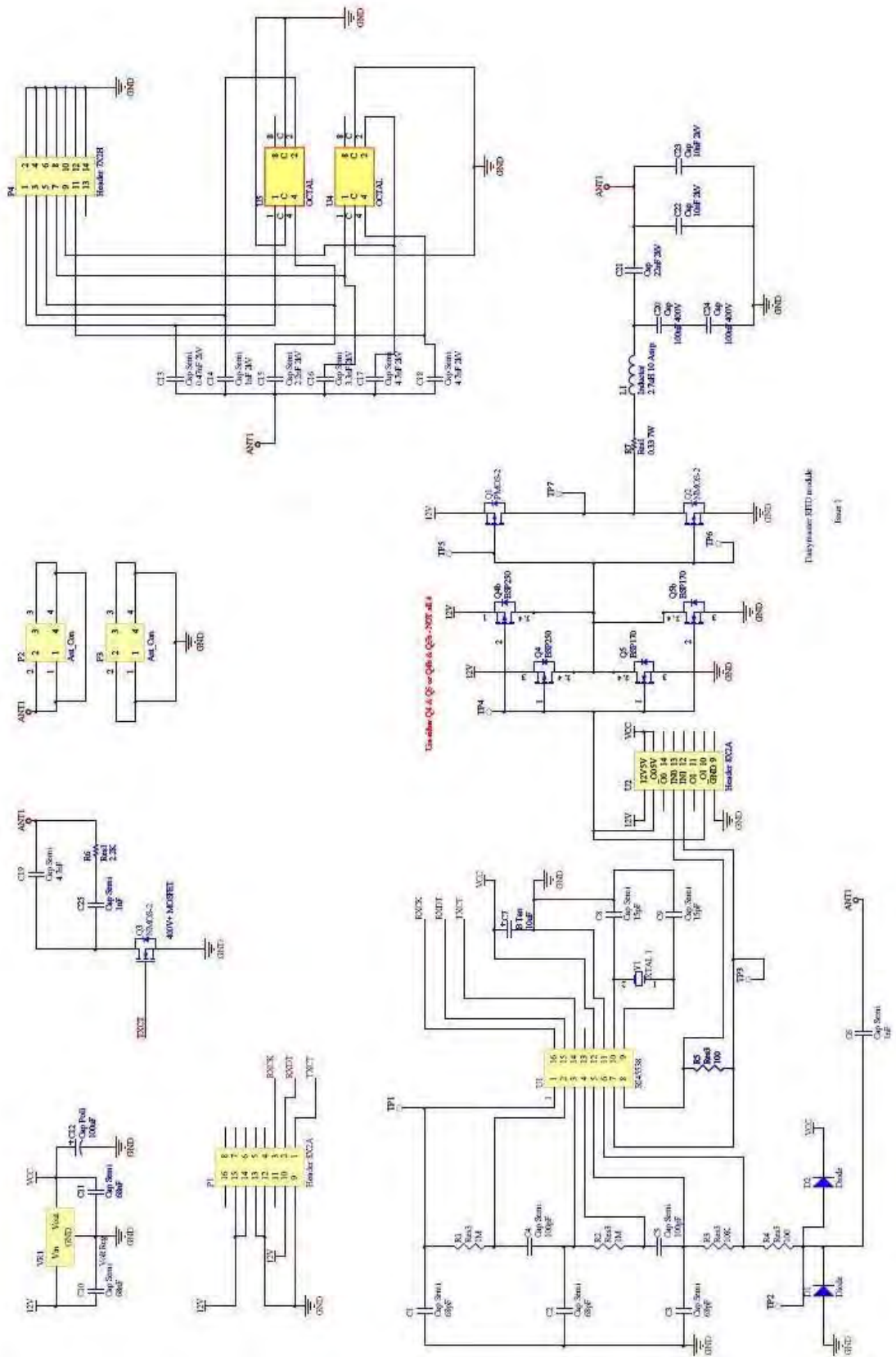


Figure B.3: Final Auto-ID Module Schematic (Also see Appendix A.5)